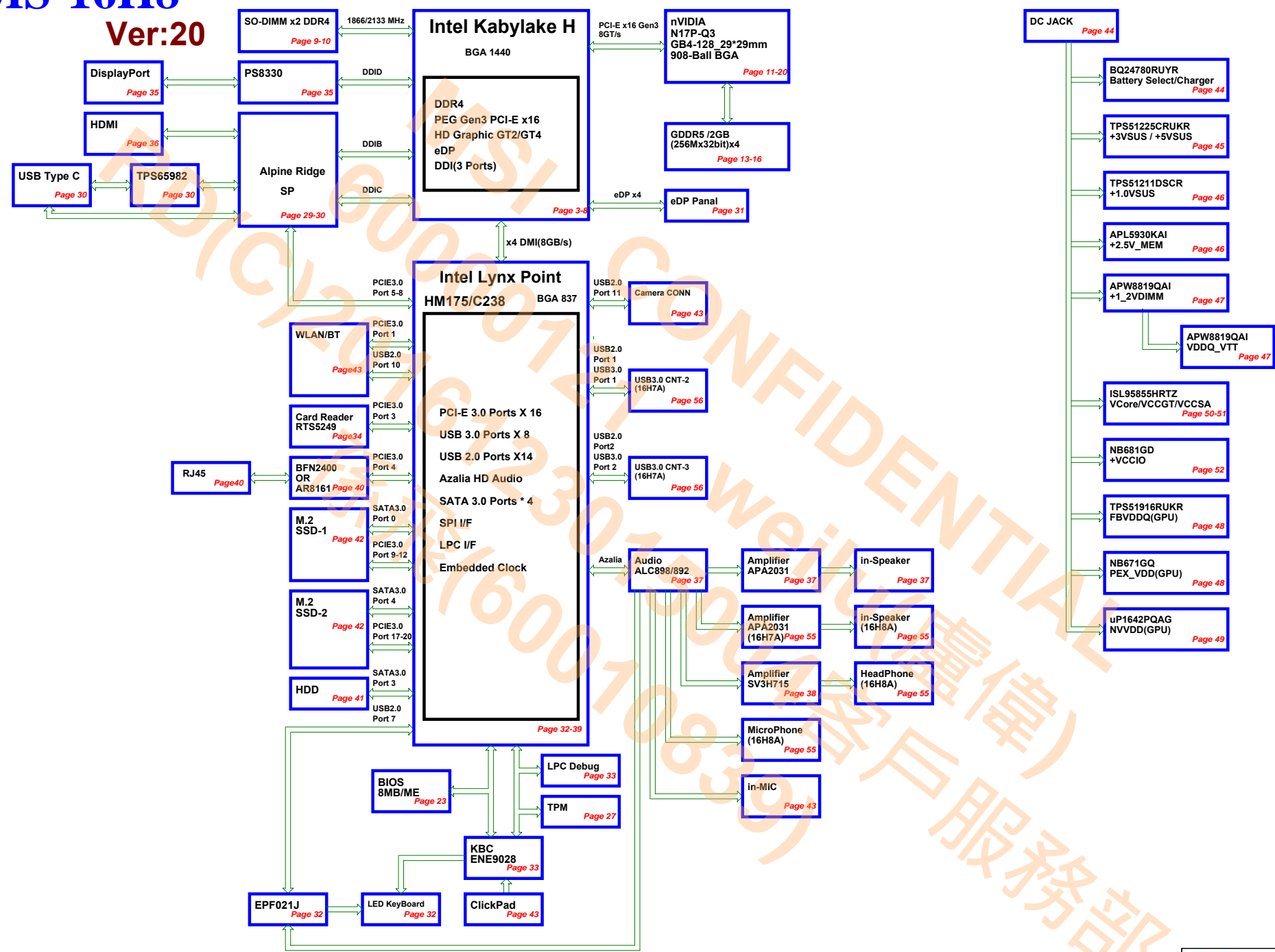
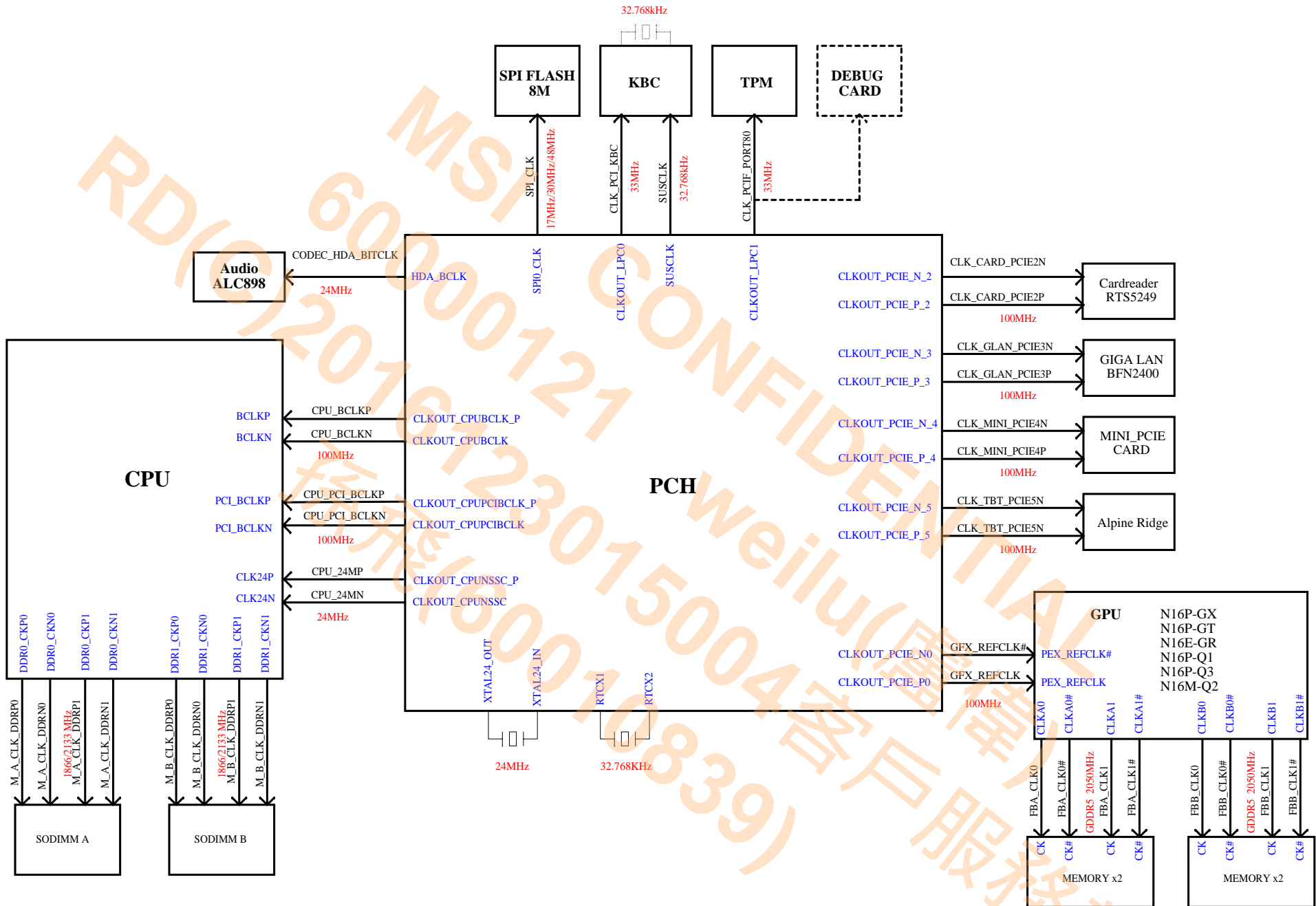


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Ver:20

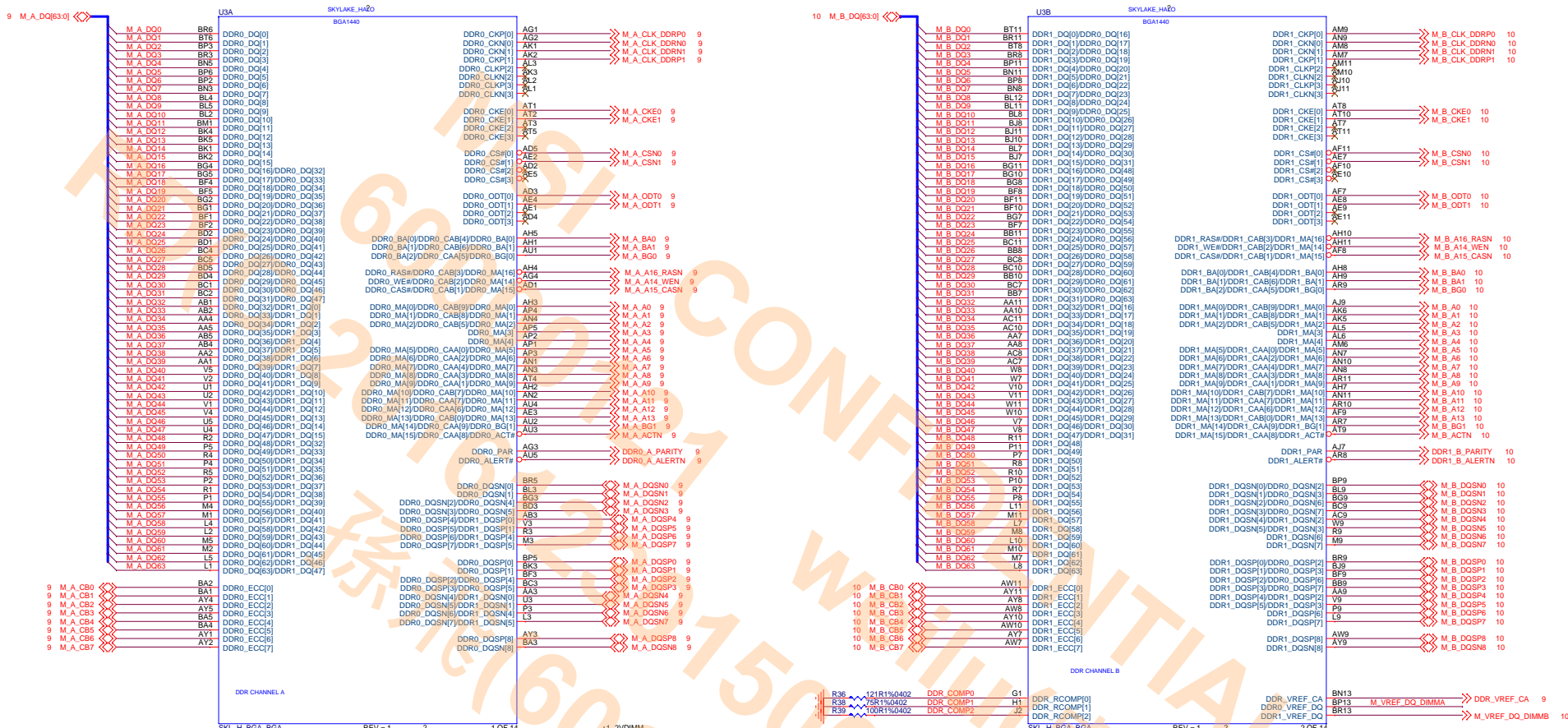
Intel Kabylake Platform

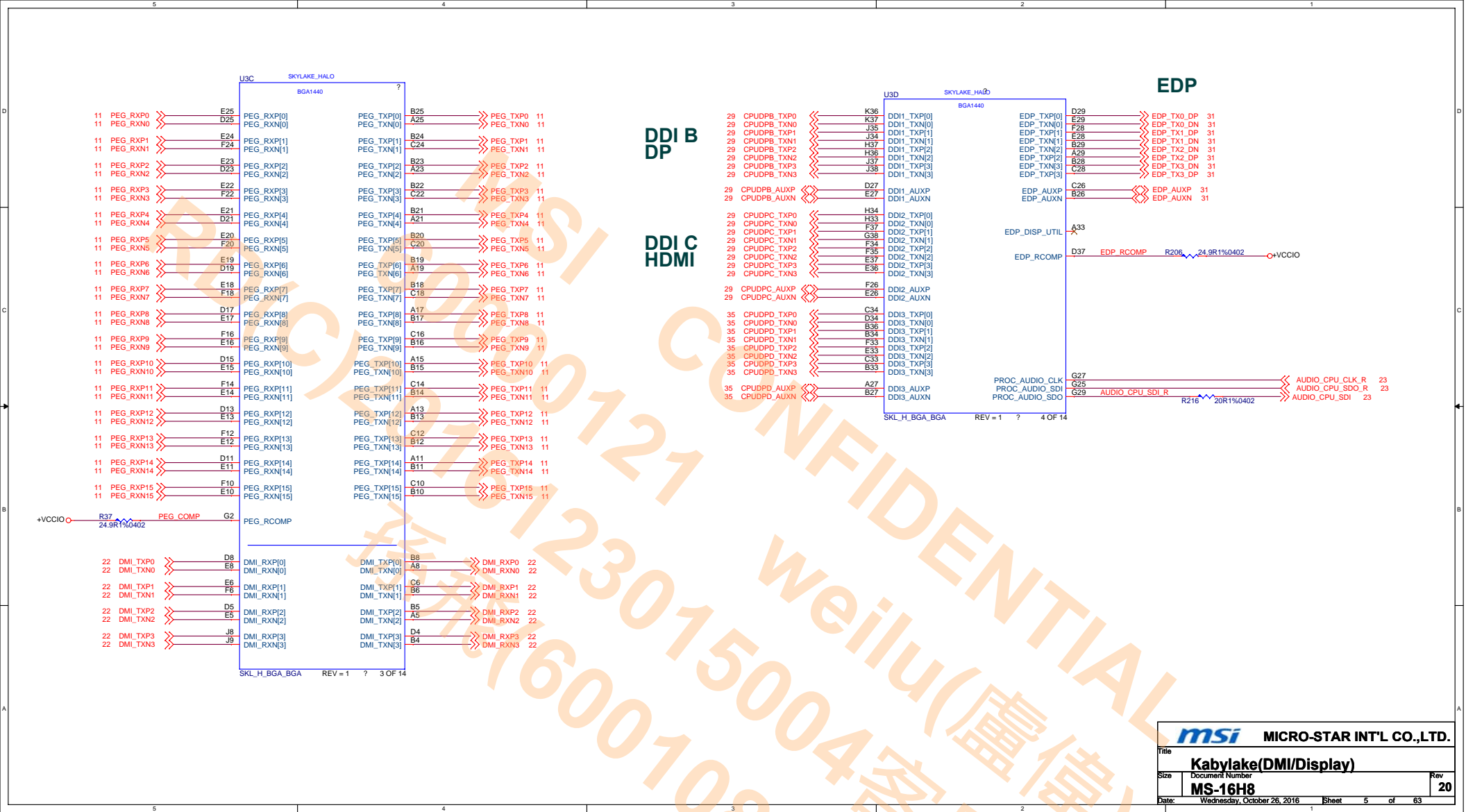


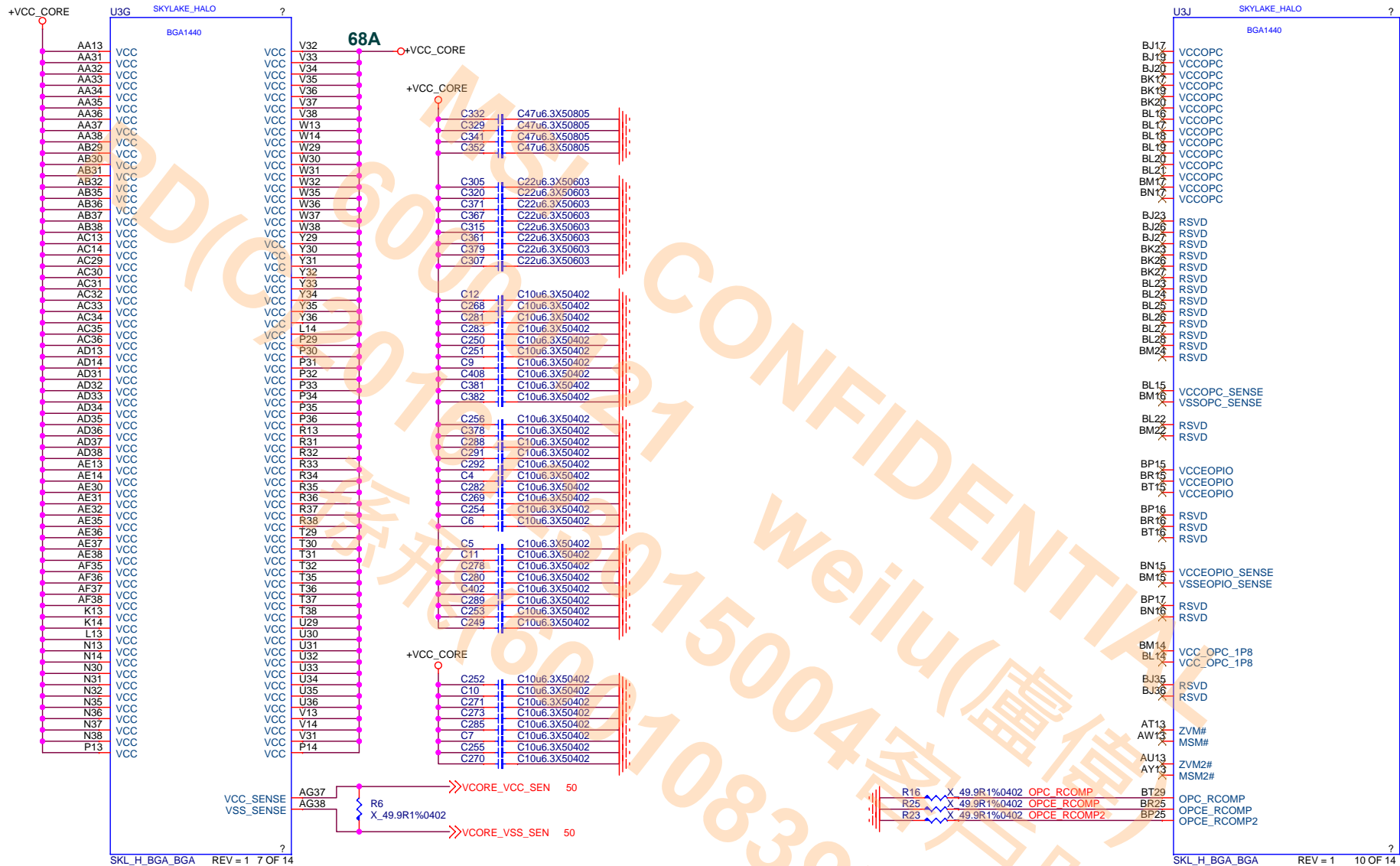


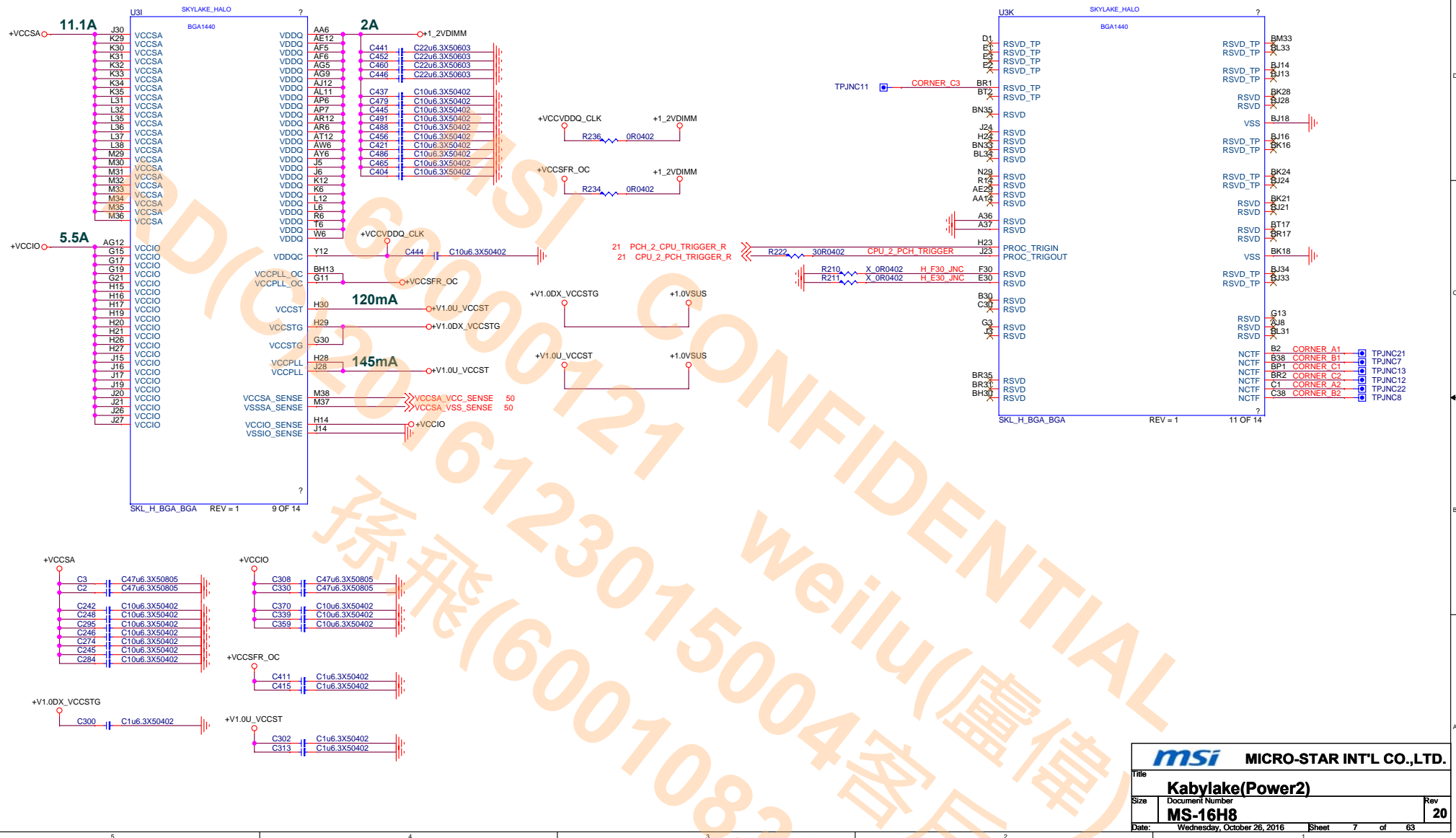
DDR Channel A

DDR Channel B

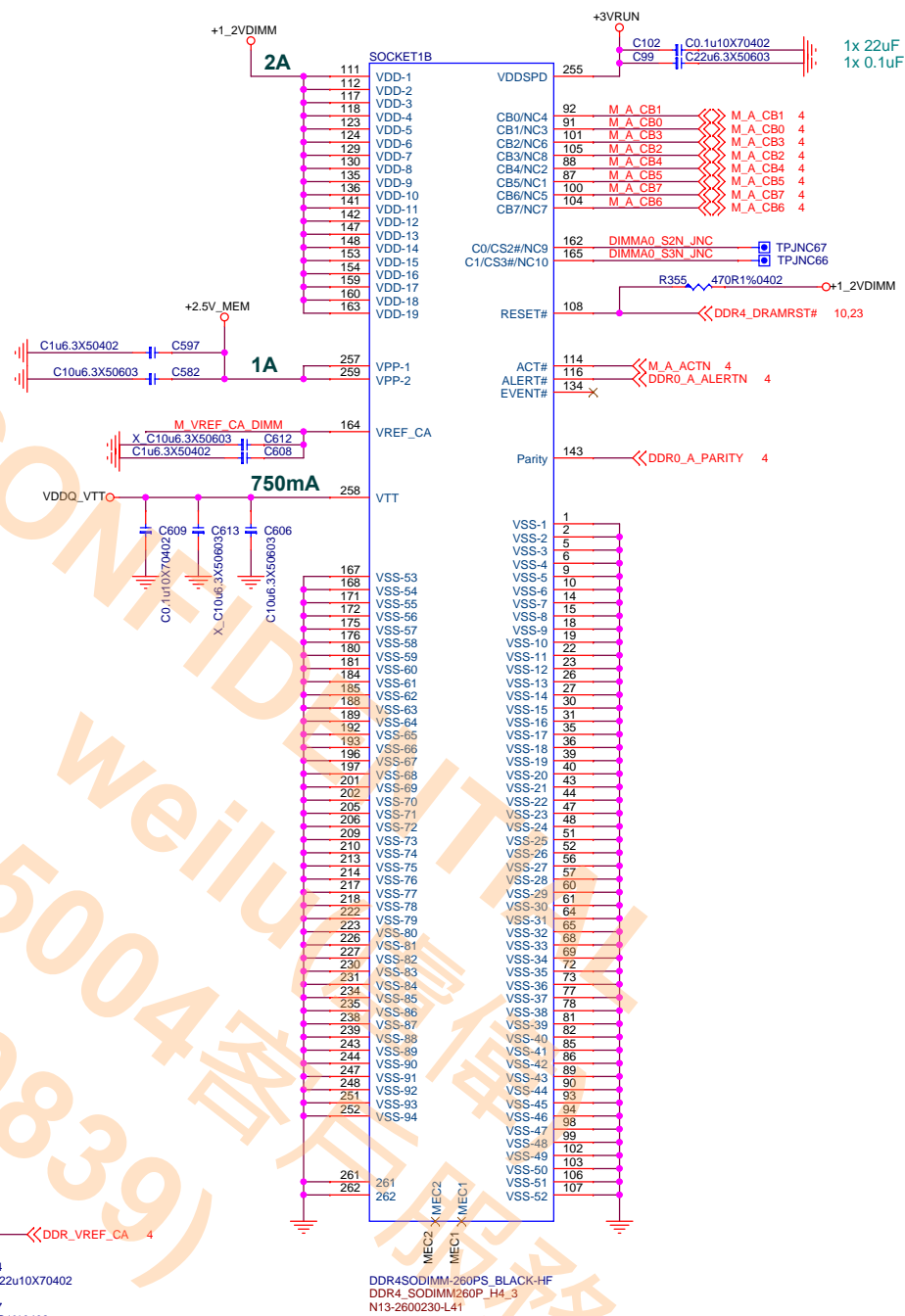
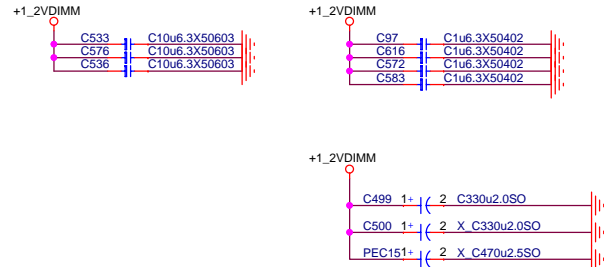




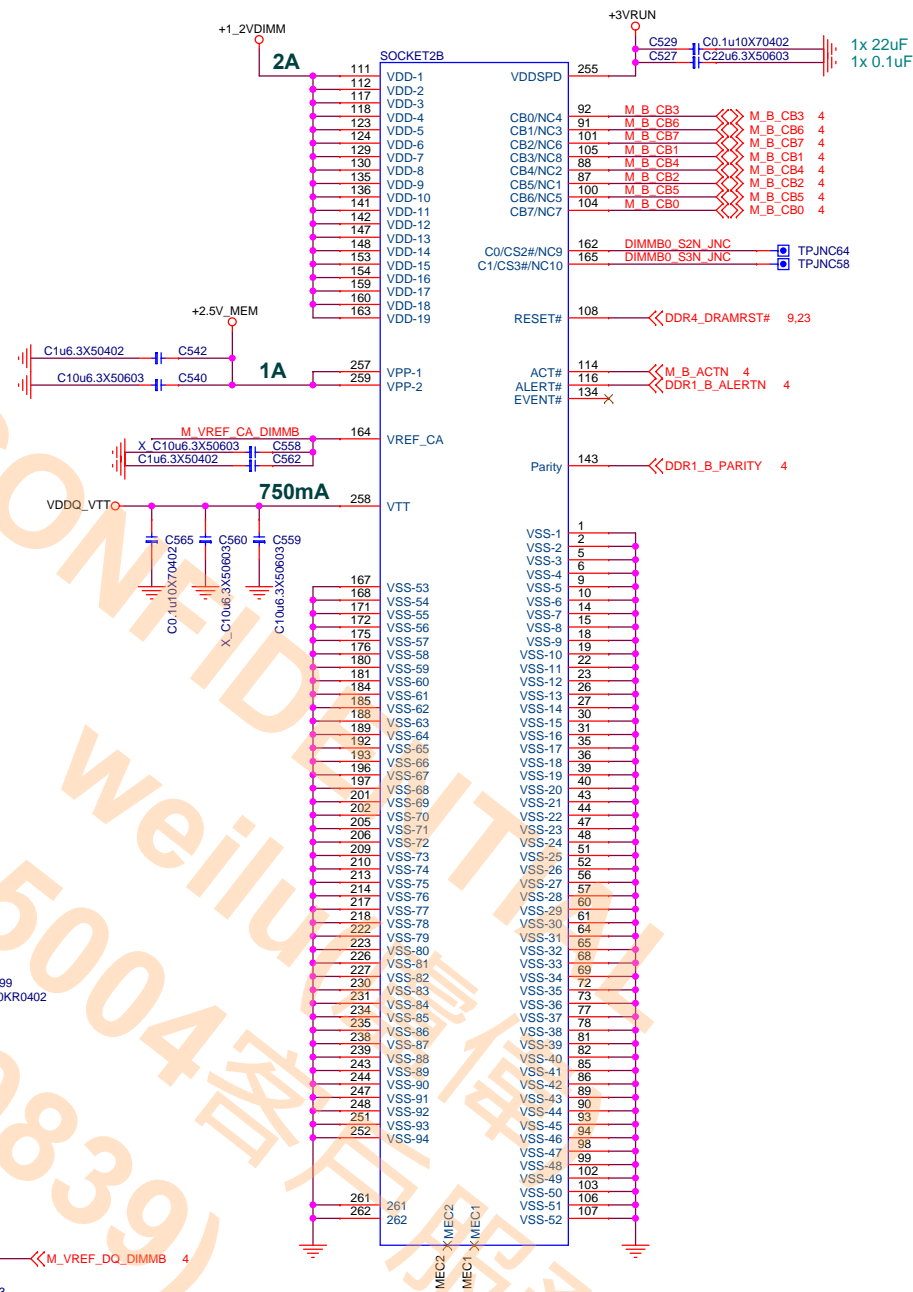
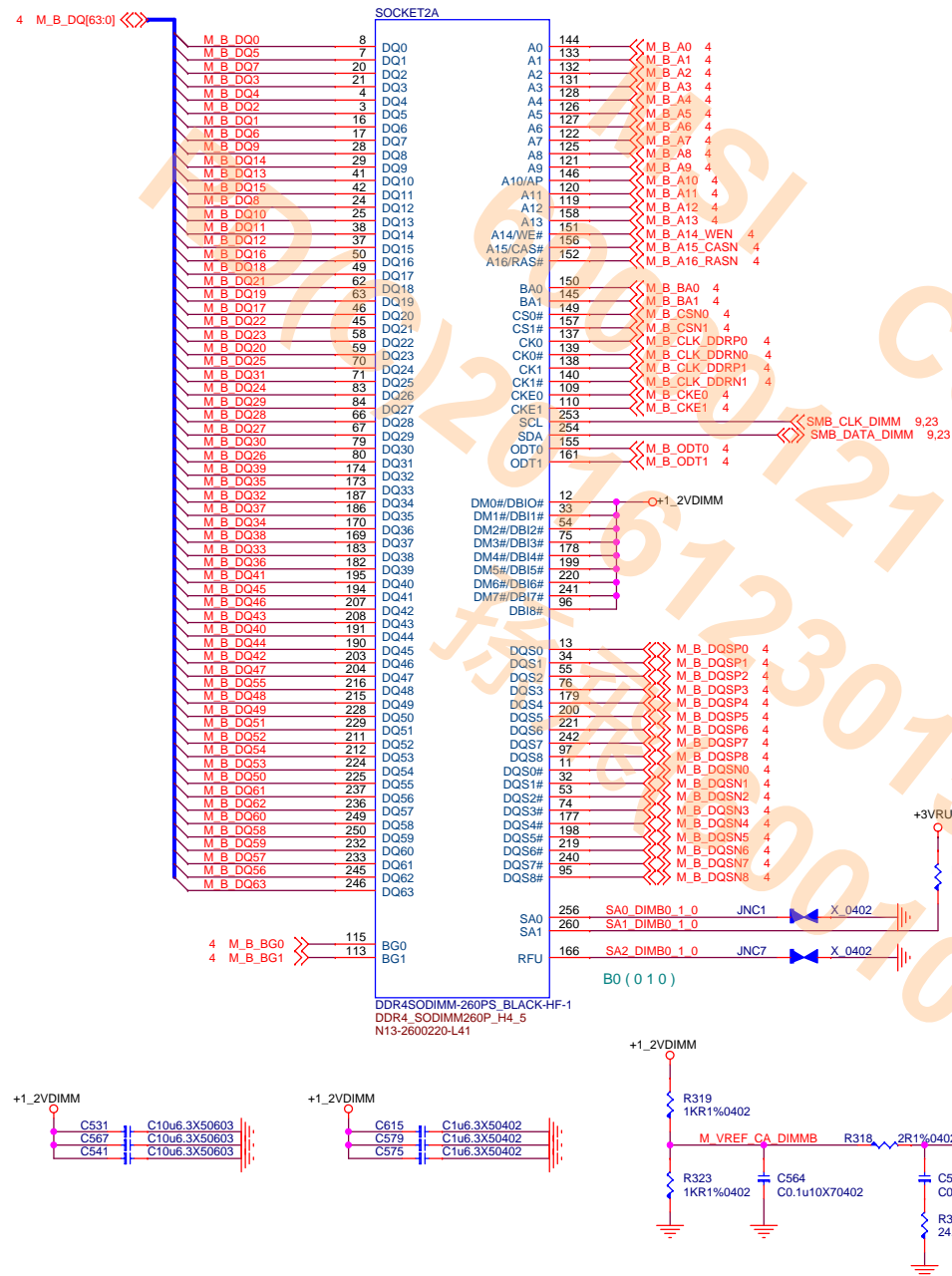




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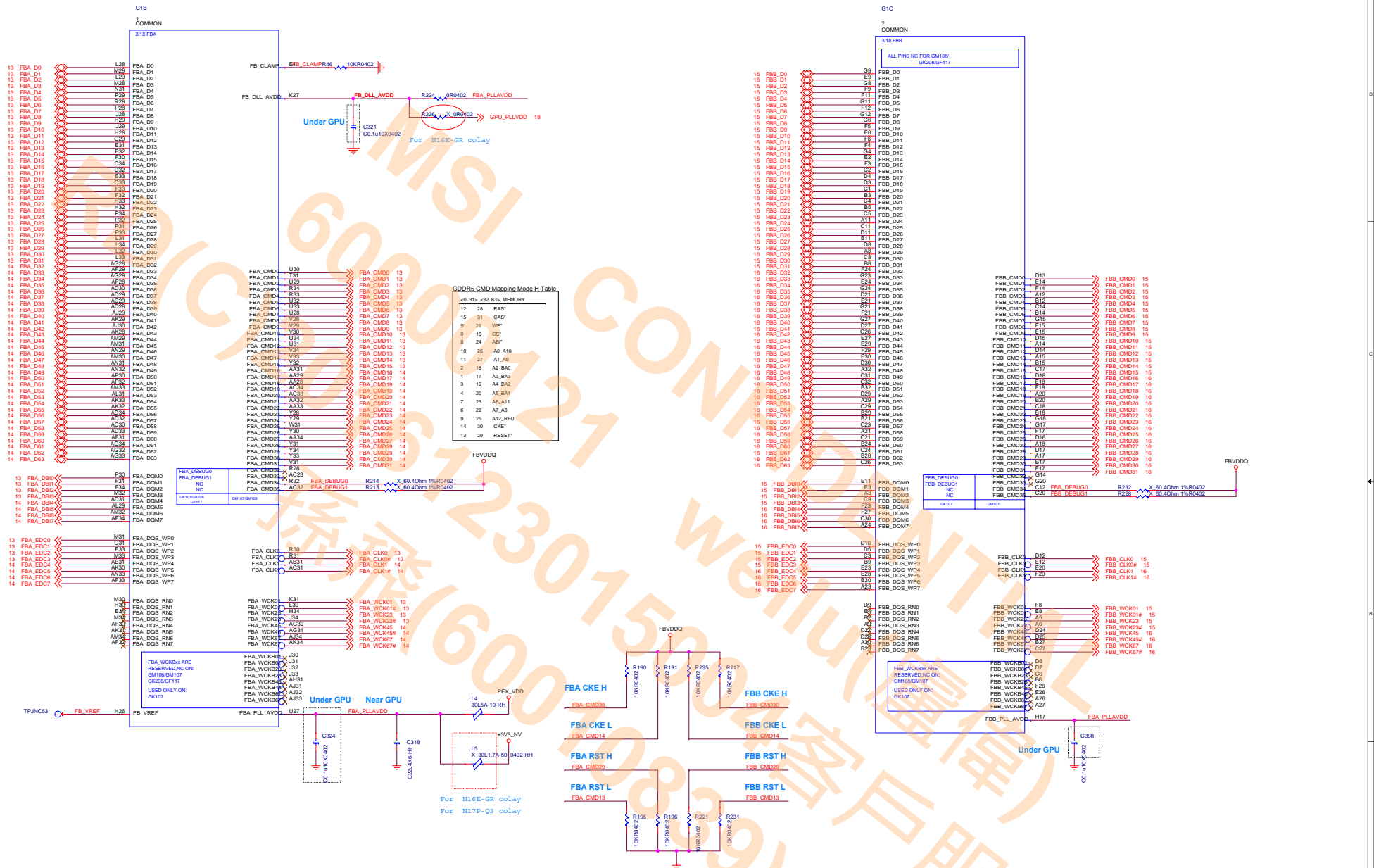


SODIMM_B0

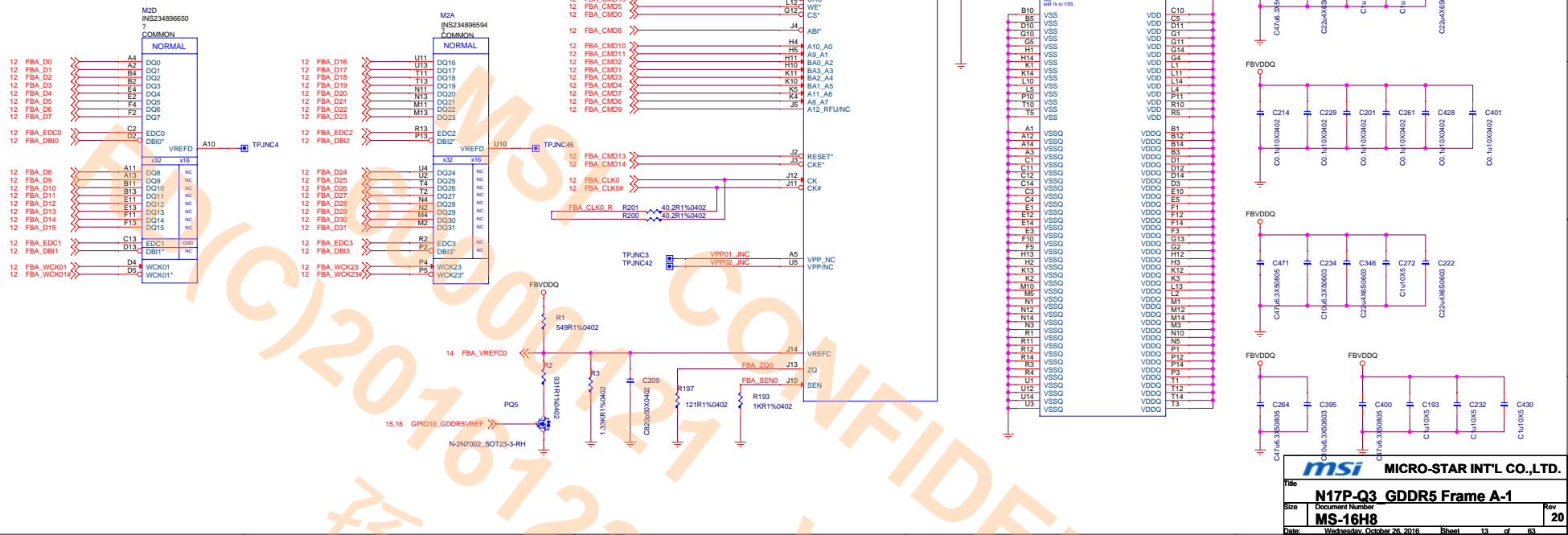


18,20,24,33 DGPU_PWRGD >> G N-2N7002LT1G_SOT23-RH
PEX_CLKREQ#

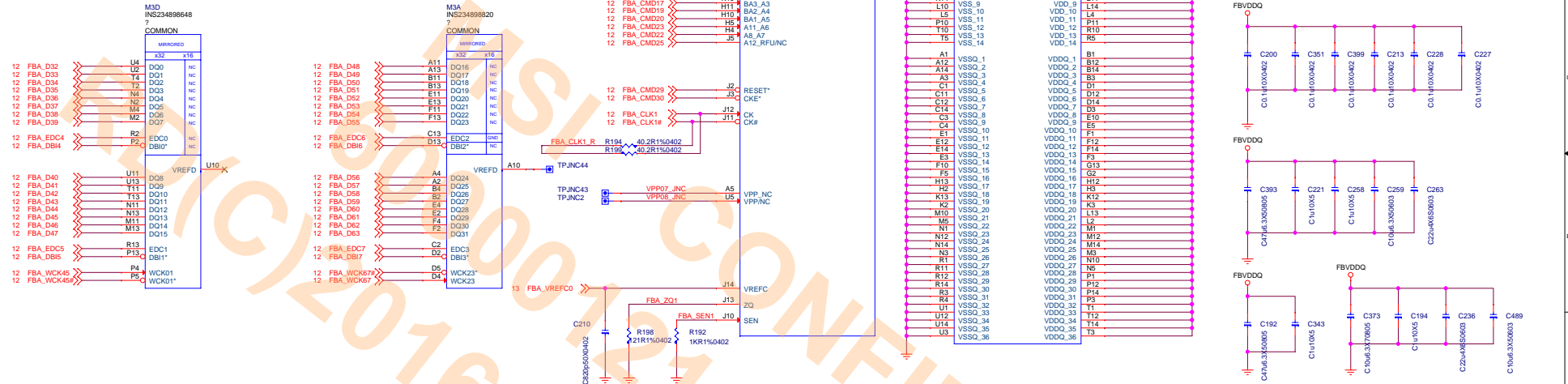
N16P-GX (Frame Buffer Interface)



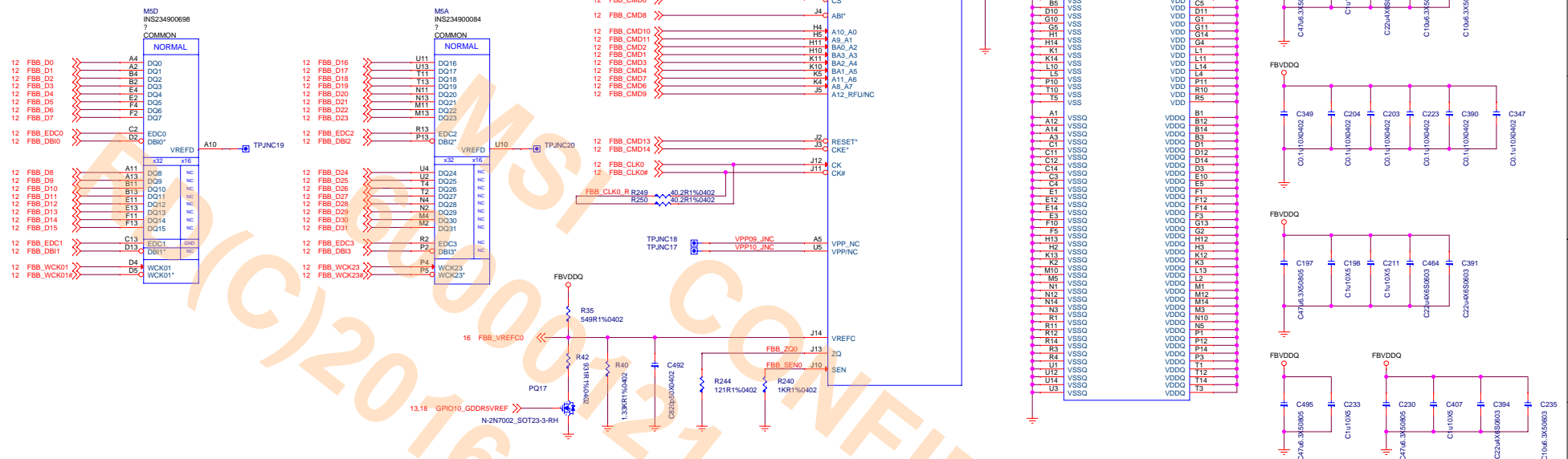
N16P_GX(GDDR5 Frame A-1)



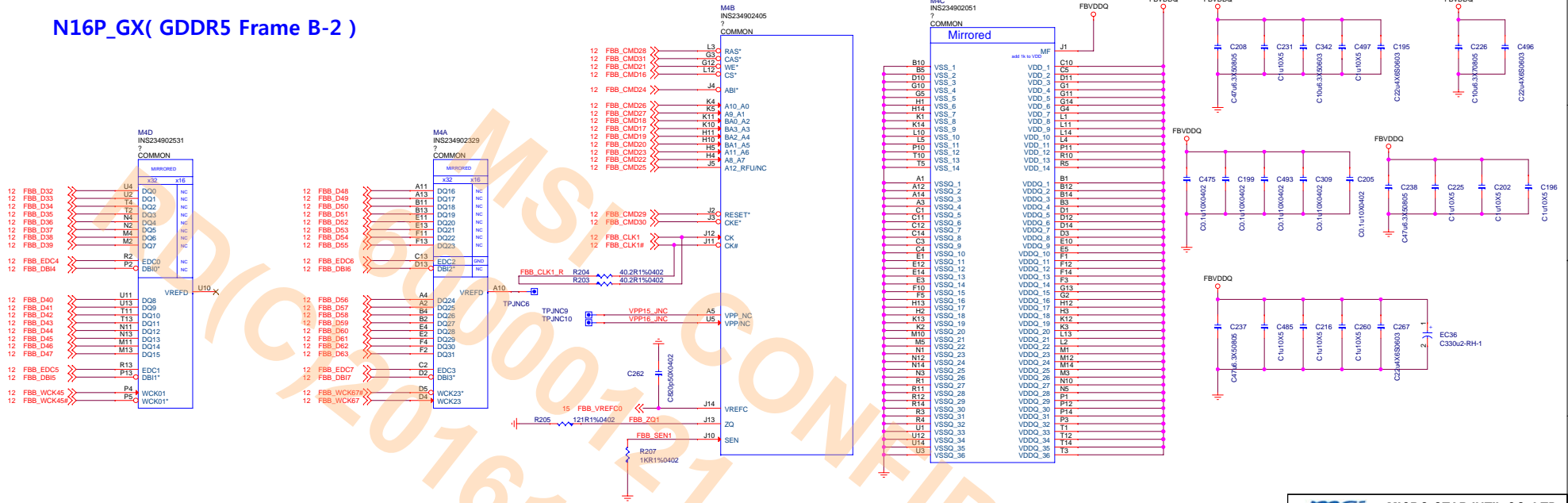
N16P_GX(GDDR5 Frame A-2)



N16P_GX(GDDR5 Frame B-1)

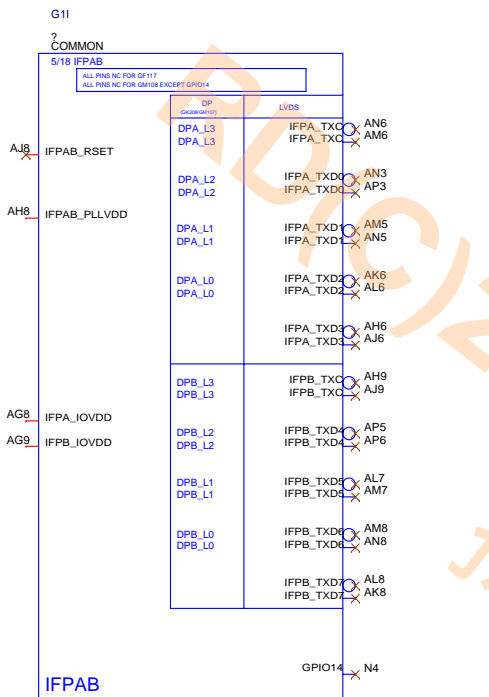


N16P_GX(GDDR5 Frame B-2)

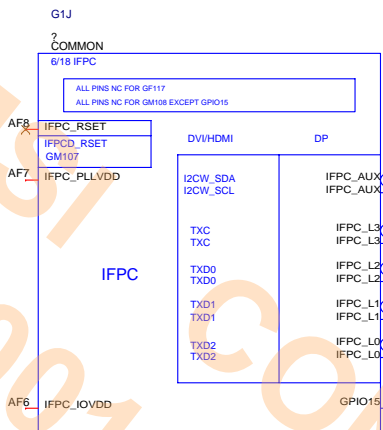


N16P-GX (Display IF)

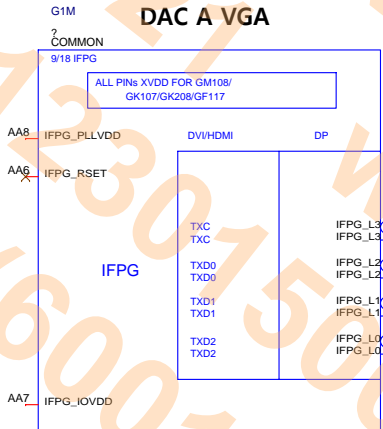
IFP A/B LVDSDual Link



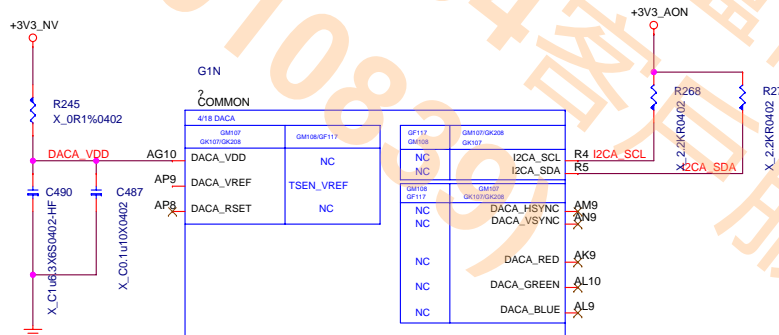
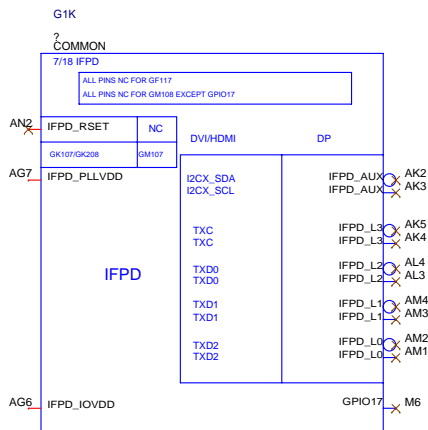
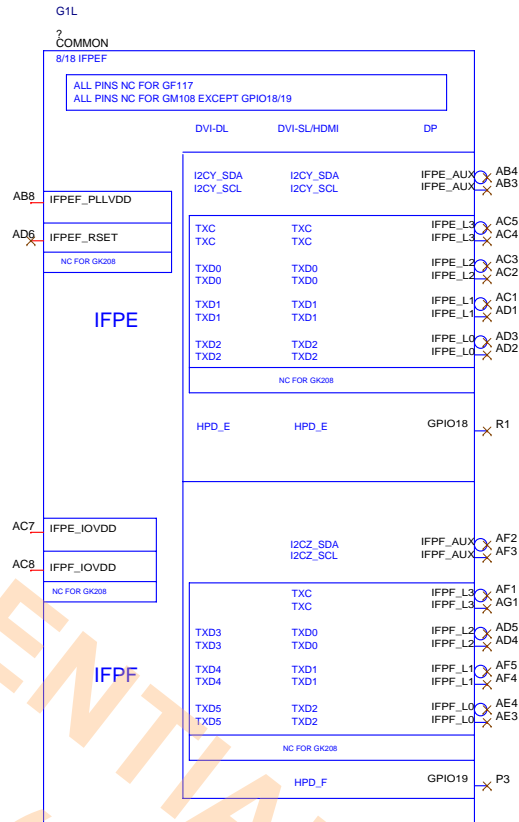
IFP C Native HDMI OR DP



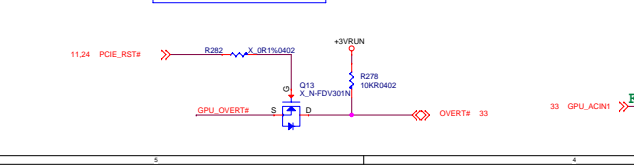
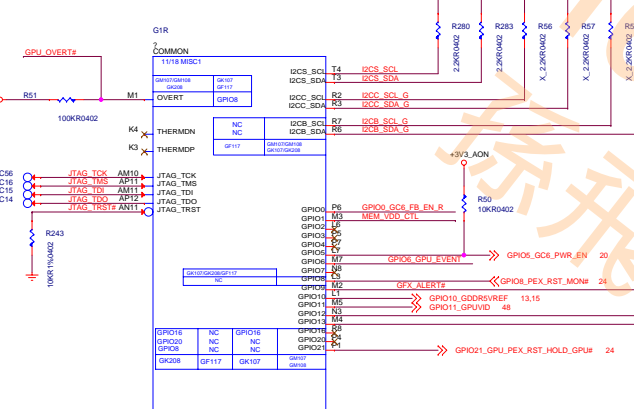
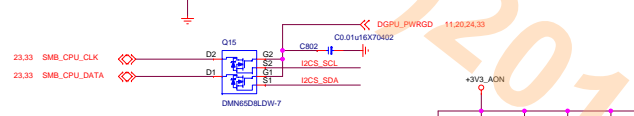
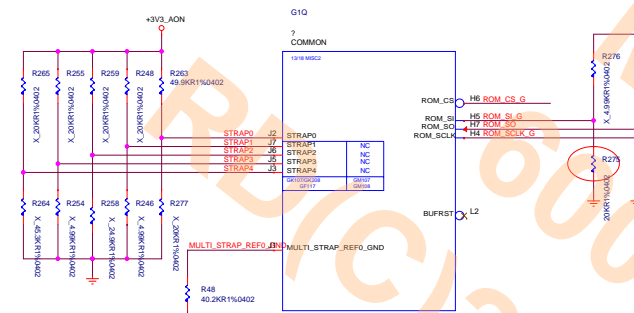
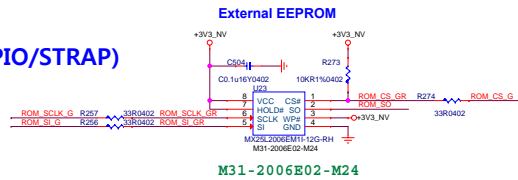
DAC A VGA



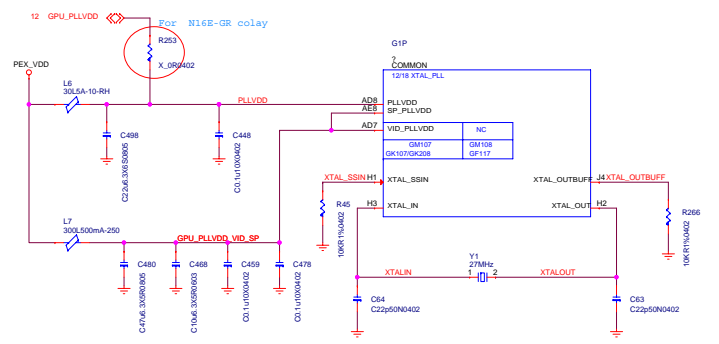
IFP E/F Dual Link TMDS DVI-I



N16P-GX (GPIO/STRAP)

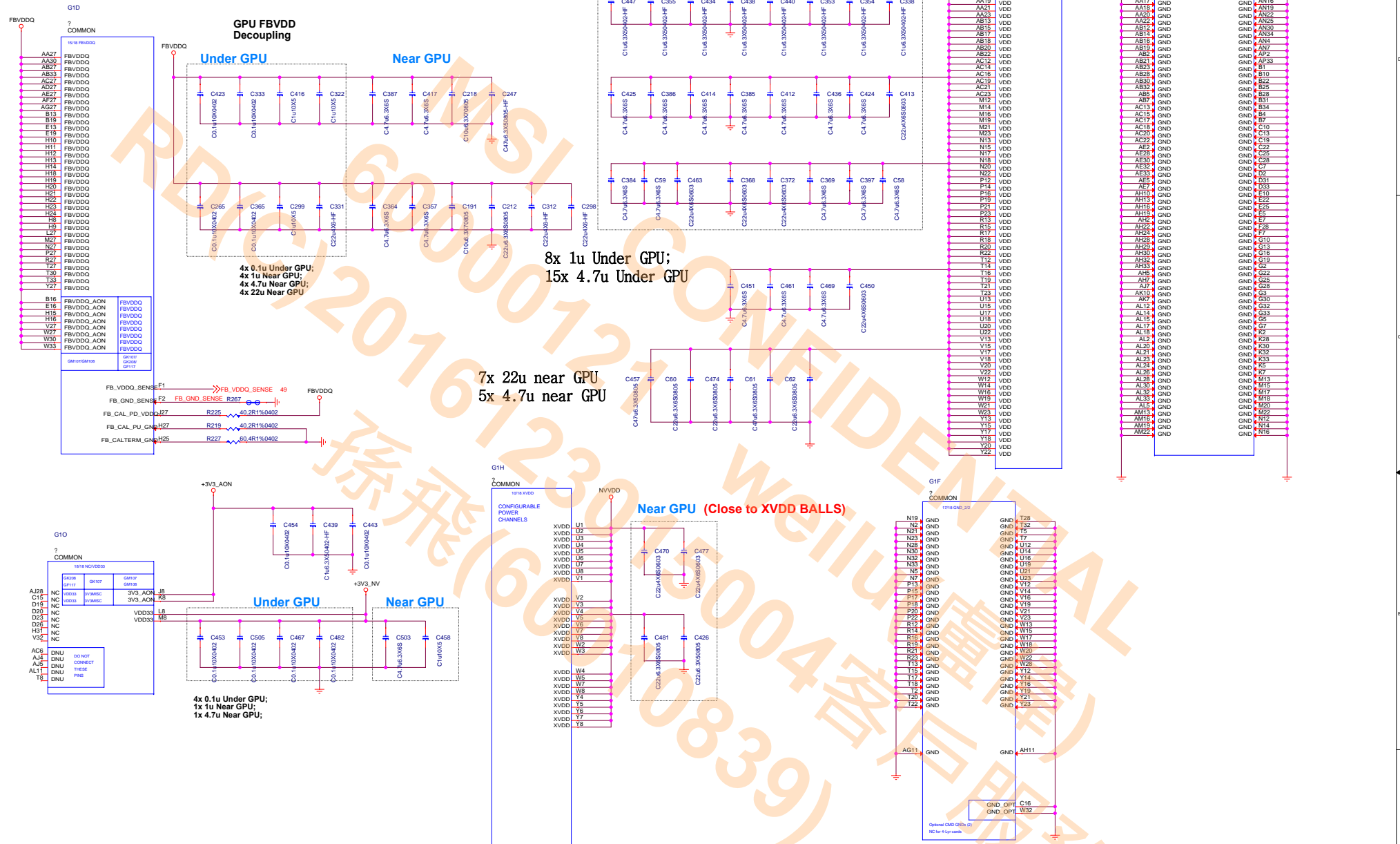


Item	Location	N17P-Q3
Strap Mode	R48	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x1436
Package		GB4B-128
Memory Type		GDDR5
ROM_S1	R275	0x3,Samsung 8G, 20kohm Pull Down K4G08325FB-HC03
	R275	0x4,Micron 8G, 24.9kohm Pull Down MT51J256M32HF-60-A
ROM_SO	R237	0x0,4.99kohm Pull Down
ROM_SCLK	R242	0x0,4.99kohm Pull Down
Strap0	R263	49.9kohm pull up to +3V3_AON
Strap1	R248 R246	Do no stuff
Strap2	R259 R258	Do no stuff
Strap3	R255 R254	Do no stuff
Strap4	R265 R264	Do no stuff



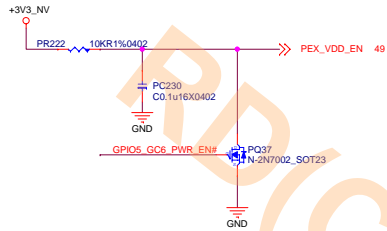
Pin Name	Normal function	I/O	Functional Description	
GP100	GC6_FB_EN	O	FB Enable GC62.0	10K PD
GP101	MEM_VDD_CTL	O	Memory Voltage Control	PURV_PD to set
GP102	NC_LCD_BL_PWM	O	Panel Backlight PWM	100K PD
GP103	NC_LCD_FWR_EN	O	Panel power Enable	100K PD
GP104	NC_LCD_BL_EN	O	Panel Backlight Enable	100K PD
GP105	GC6_PWR_EN	O	GPU Power Sequence for GC2.0	10K PU 3V3_AON
GP106	GPU_EVENT*	I	GPU Wake for GC2.0	10K PU 3V3_AON
GP107	NC_IDStereo/behg	O	3D Vision L/R Signal	100K PD
GP108	SYS_PEX_RST_MON*	I	SYS Side PCIe reset monitor	10K PU 3V3_AON
GP109	ThermAlert*/ERR	I/O	Thermal ALERT	10K PU 3V3_AON
GP1010	GDDR5VREF	O	Memory VREF Control	100K PD
GP1011	GP1011_GPUVID	O	GPU Core VDD PWM control signal	
GP1012	GPU_ACTIN	I	AC power detect	100K PU 3V3_AON
GP1013	FBVREF_PSI#	O	Phase Shedding	
GP1014	NC	I	Hot plug detect for IFPA	
GP1015	NC	I	Hot plug detect for IFPC	
GP1016	NC	O		
GP1017	NC	I	Hot plug detect for IFPD	
GP1018	NC	I	Hot plug detect for IFPE	
GP1019	NC	I	Hot plug detect for IFPF	
GP1021	SPU_PEX_RST_HOLD_GPU#	O	GPU PCIe self-reset contrl	10K PU 3V3_AON
OVER	OVERT	I/O	Catastrophic over temp	100K PU 3V3_AON

N16P-GX(Power & GND)

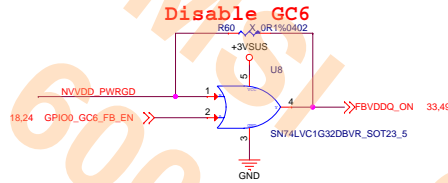


DGPU_Power Control

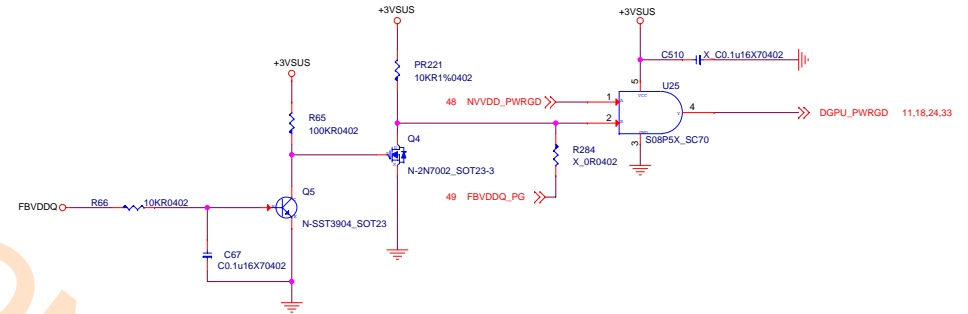
PEX_VDD_EN



FBVDDQ_ON

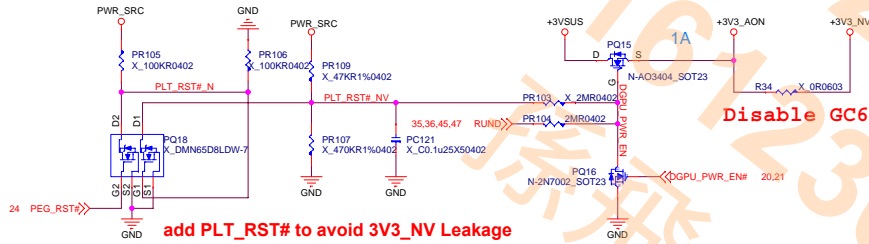


DGPU_PWRGD

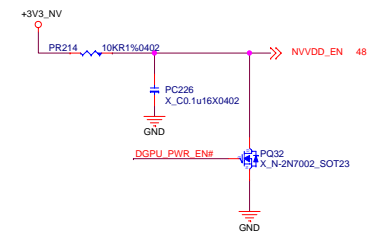


nVIDIA Power Sequence Control 3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD

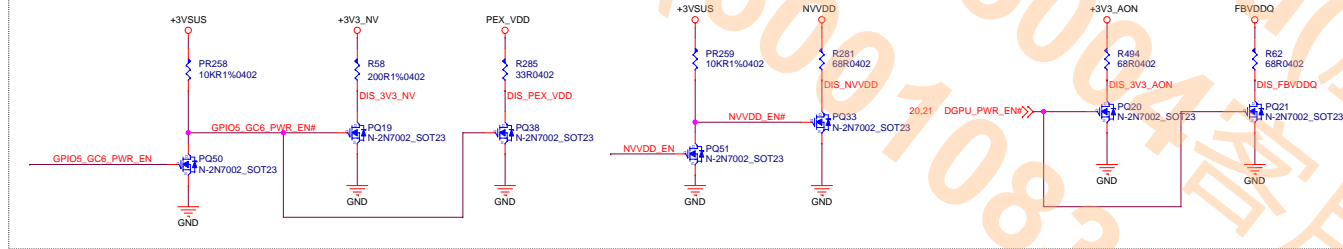
+3V3_NV

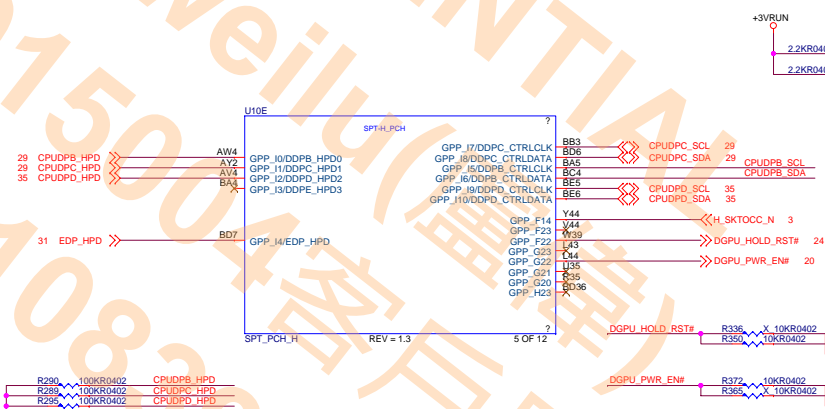
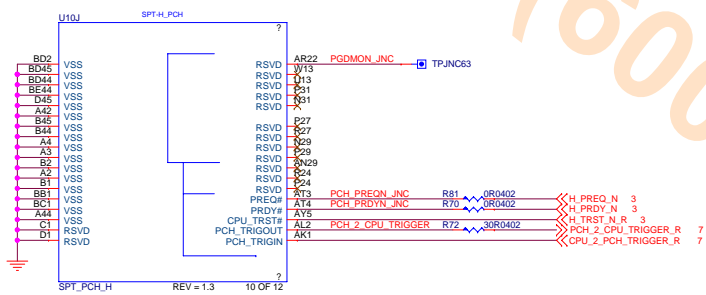
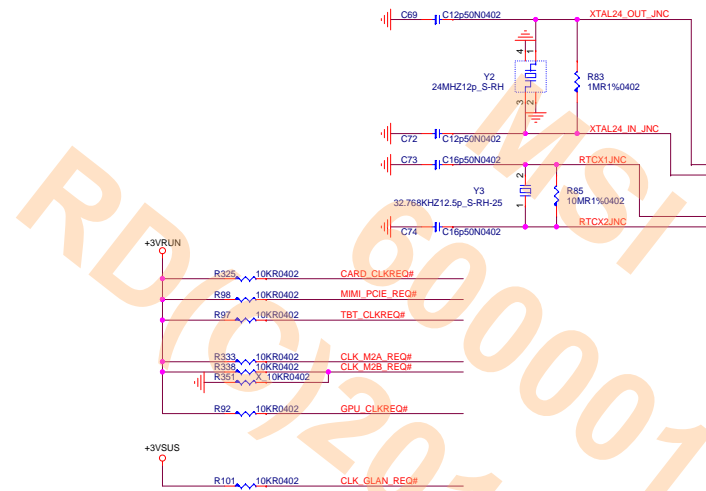


NVVDD_EN



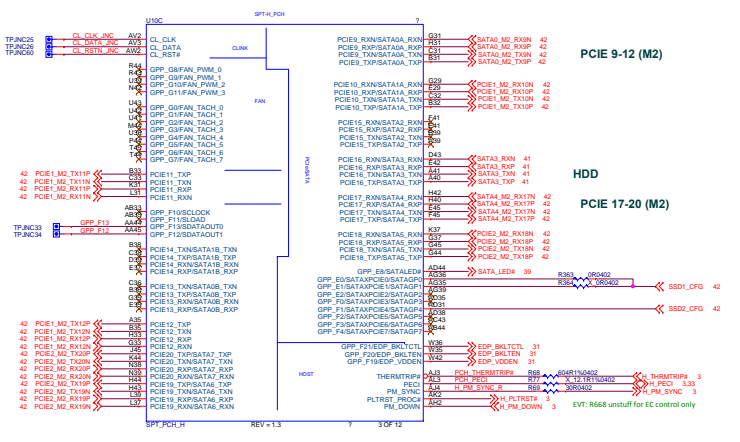
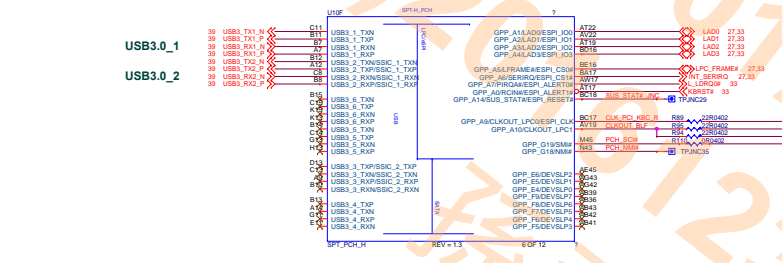
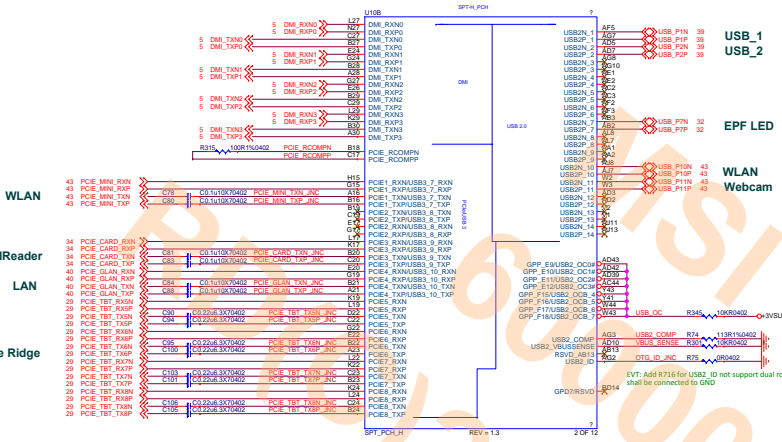
Discharge Circuit



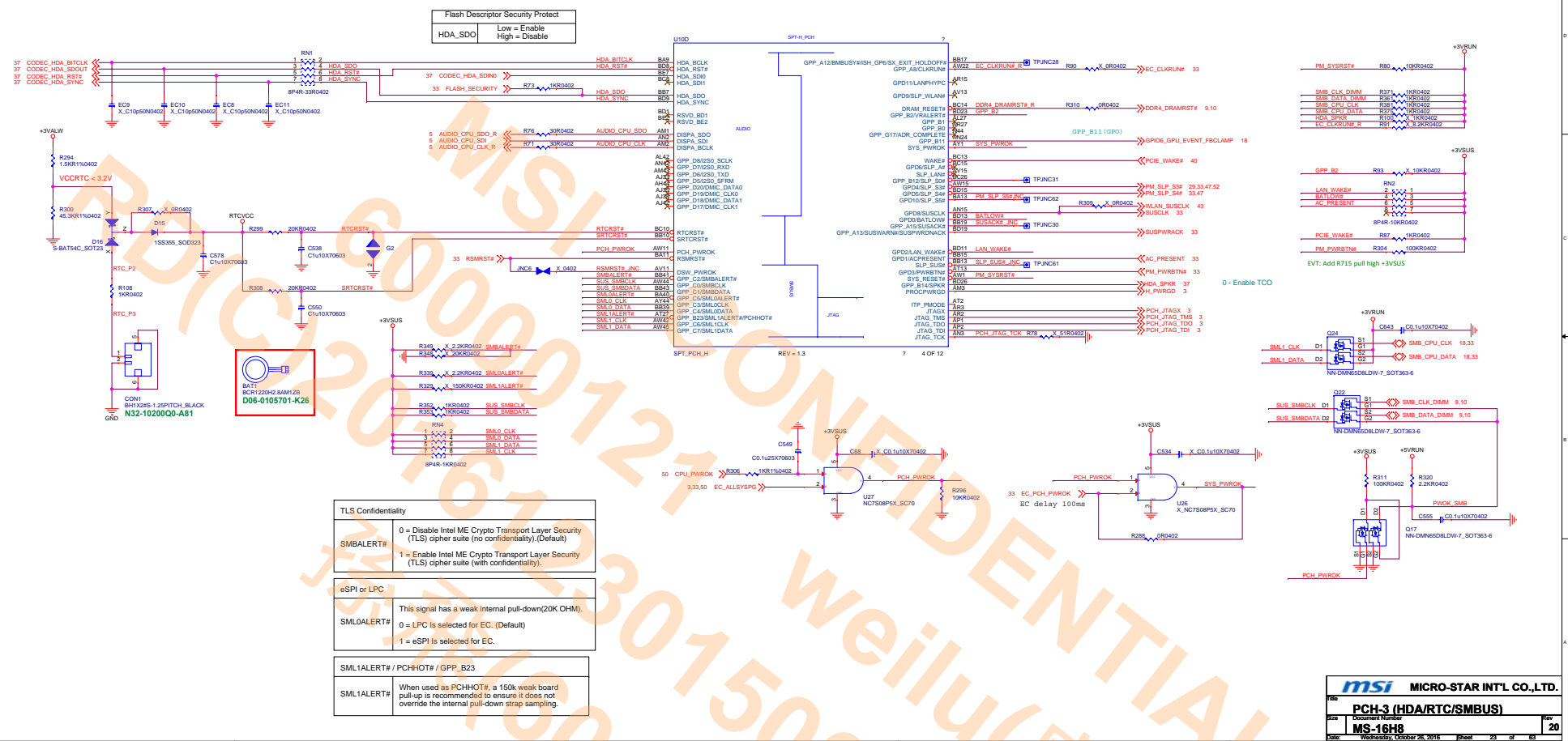


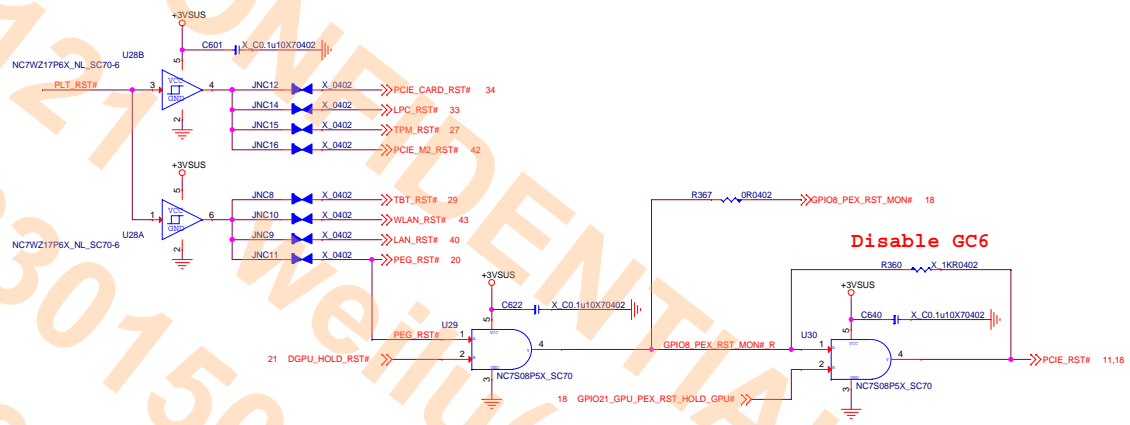
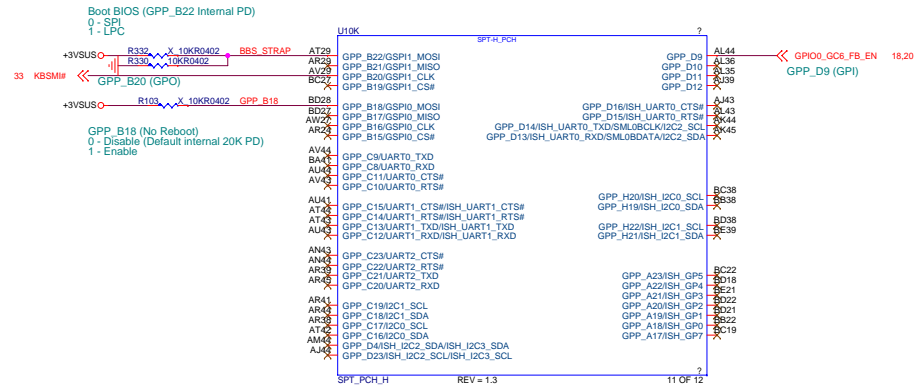
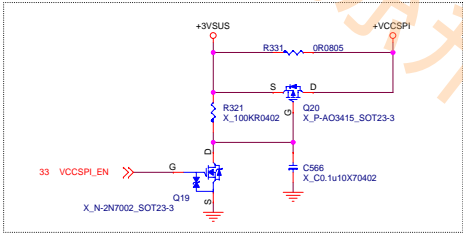
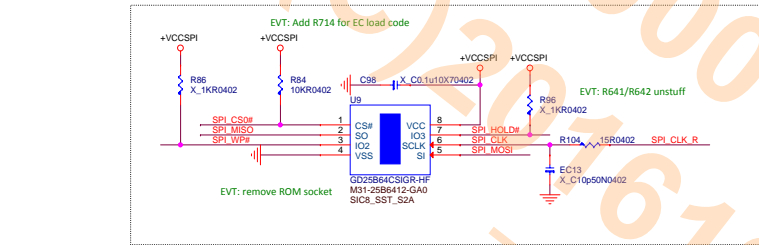
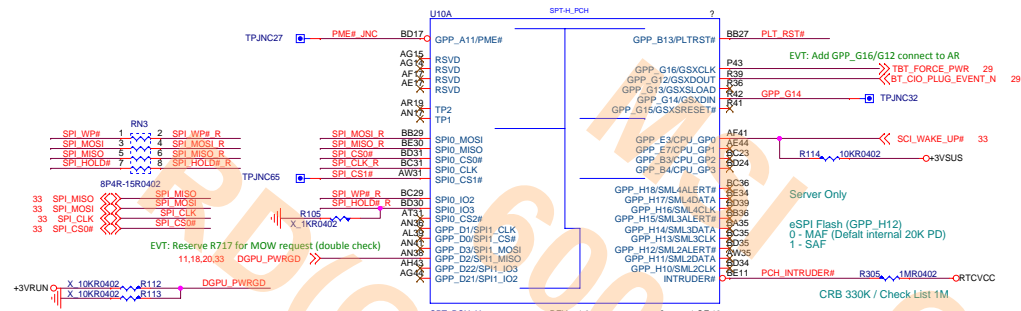
Signal	GPIO Assignment
DGPU_PWR_EN#	GPP_G22
DGPU_PWROK	NA
DGPU_HOLD_RST#	GPP_F22

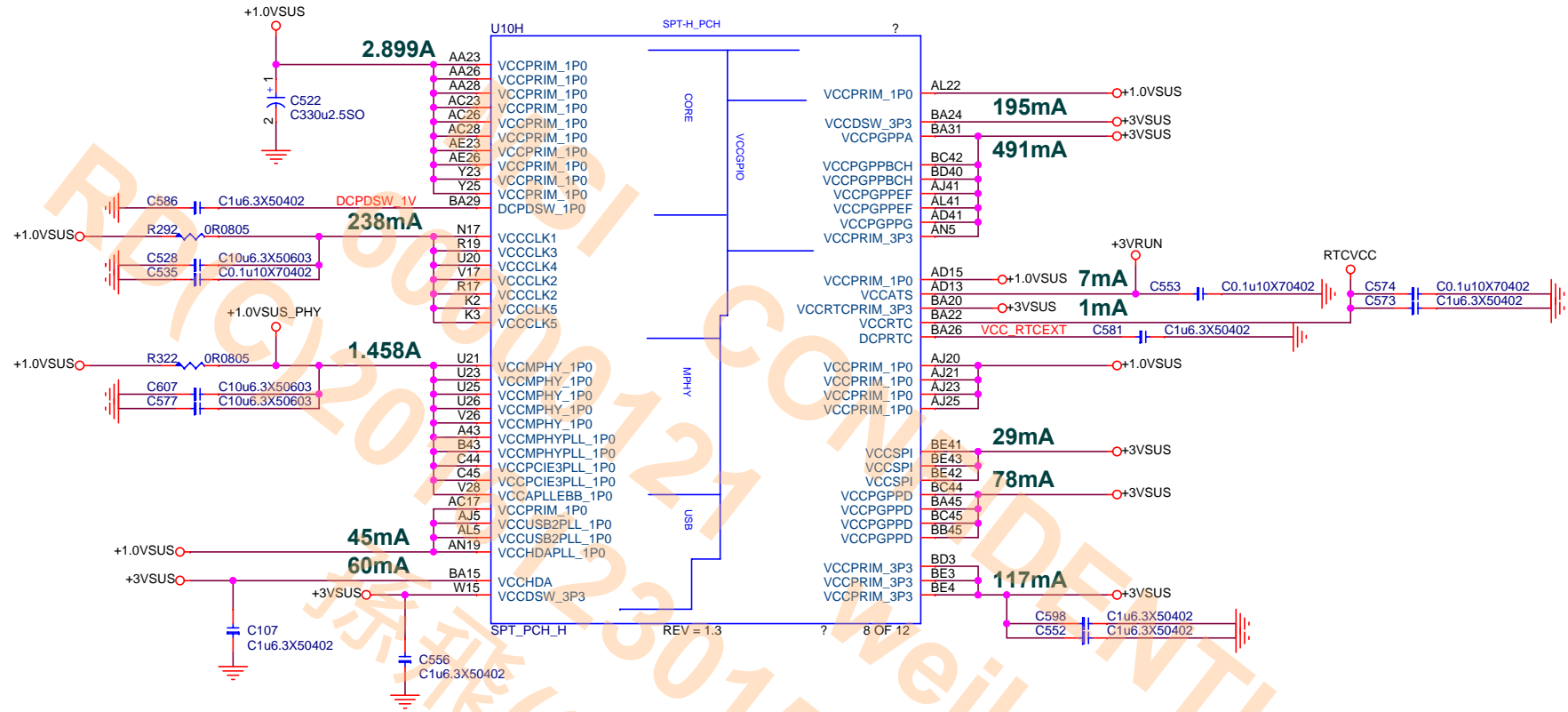
USB 2.0	USB 3.0	Device	Note
1	1	USB 3.0 Port 1	16H7A
2	2	USB 3.0 Port 2	16H7A
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8			NC
9			NC
10		WLAN	
11		WebCam	
12			NC
13			NC
14			NC

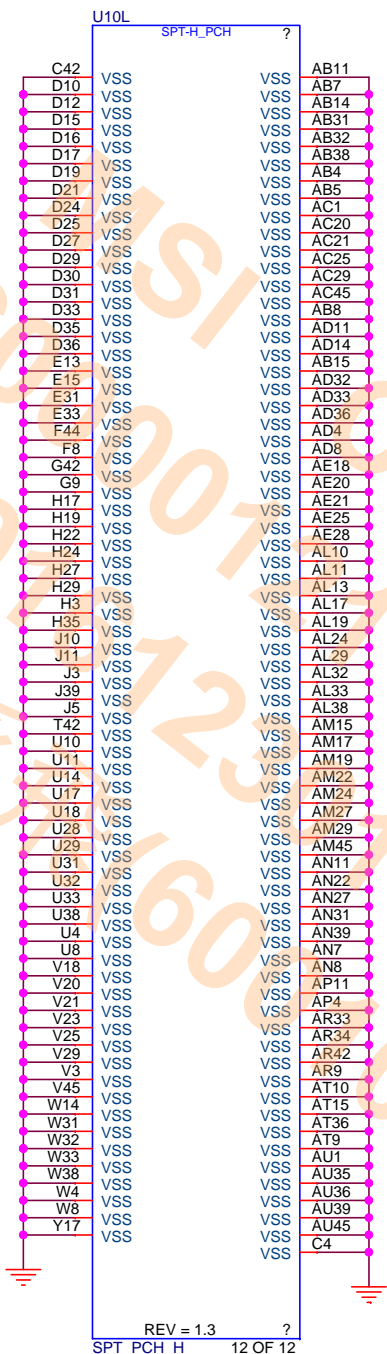
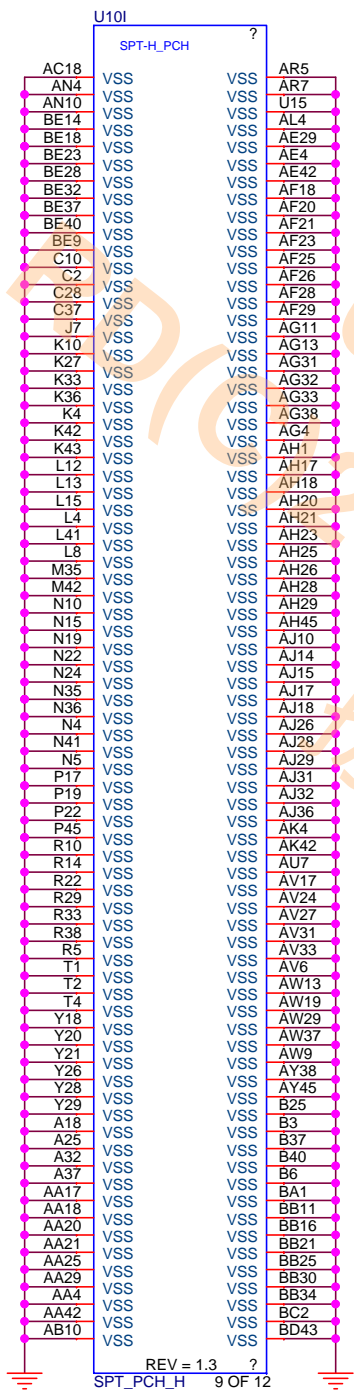


High Speed I/O Ports			
Port	Device	Device	Device
1	USB3.0/PCIe	USB3.0/PCIe	WLAN
2	USB3.0/PCIe	USB3.0/PCIe	NC
3	PCIe	USB3.0/PCIe	CardReader
4	PCIe	USB3.0/PCIe	LAN
5	PCIe	PCIe	Alpine Ridge
6	PCIe	PCIe	
7	PCIe	PCIe	
8	PCIe	PCIe	
9	SATA/PCIe	SATA/PCIe	
10	SATA/PCIe	SATA/PCIe	M.2 SSD 1
11	PCIe	PCIe	
12	PCIe	PCIe	
13	PCIe	SATA/PCIe	NC
14	PCIe	SATA/PCIe	NC
15	SATA/PCIe	SATA/PCIe	NC
16	SATA/PCIe	SATA/PCIe	HDD
17	N/A	SATA/PCIe	
18	N/A	SATA/PCIe	
19	N/A	SATA/PCIe	M.2 SSD 2
20	N/A	SATA/PCIe	

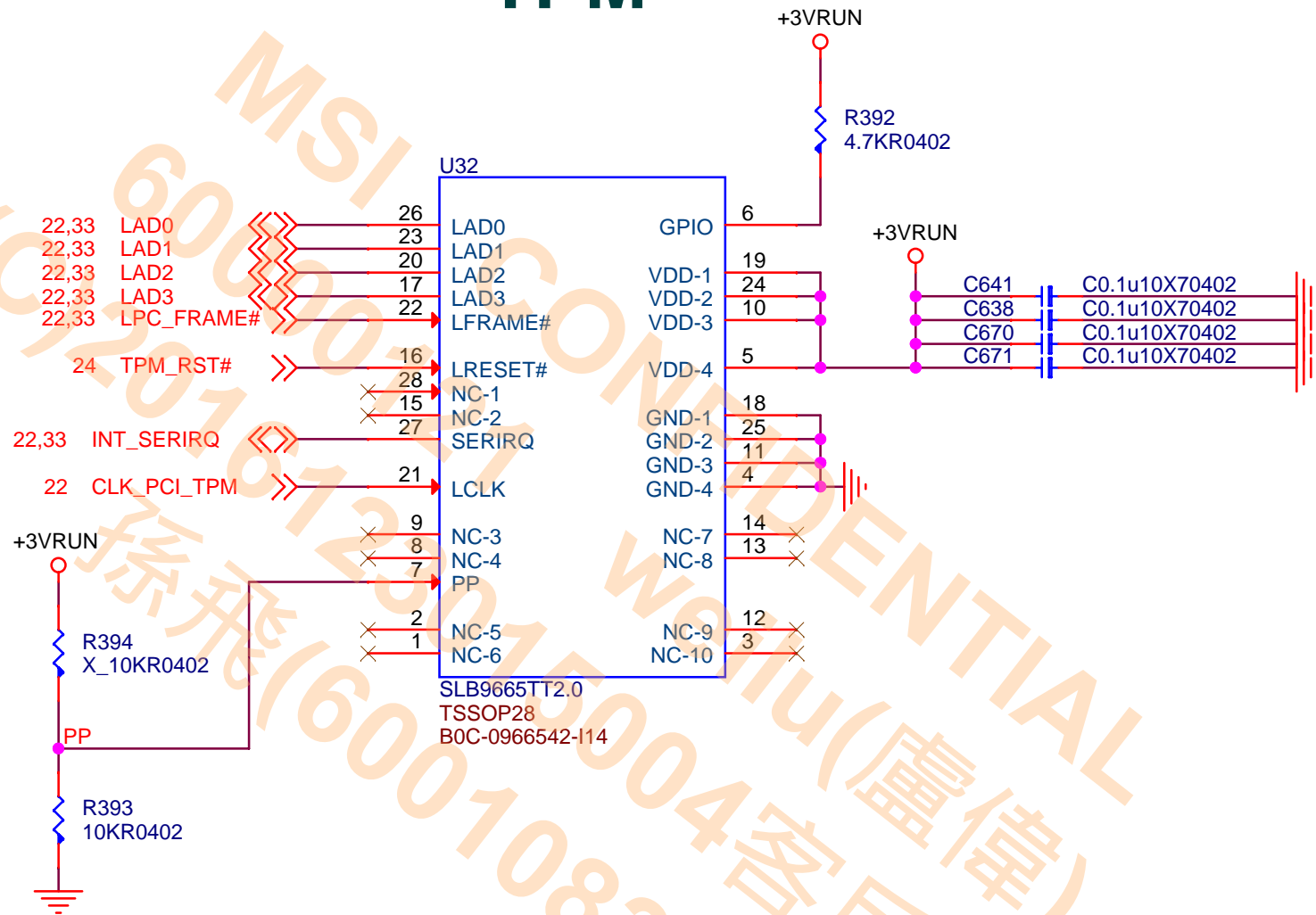








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Title

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Size

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Date:

Wednesday, October 26, 2016

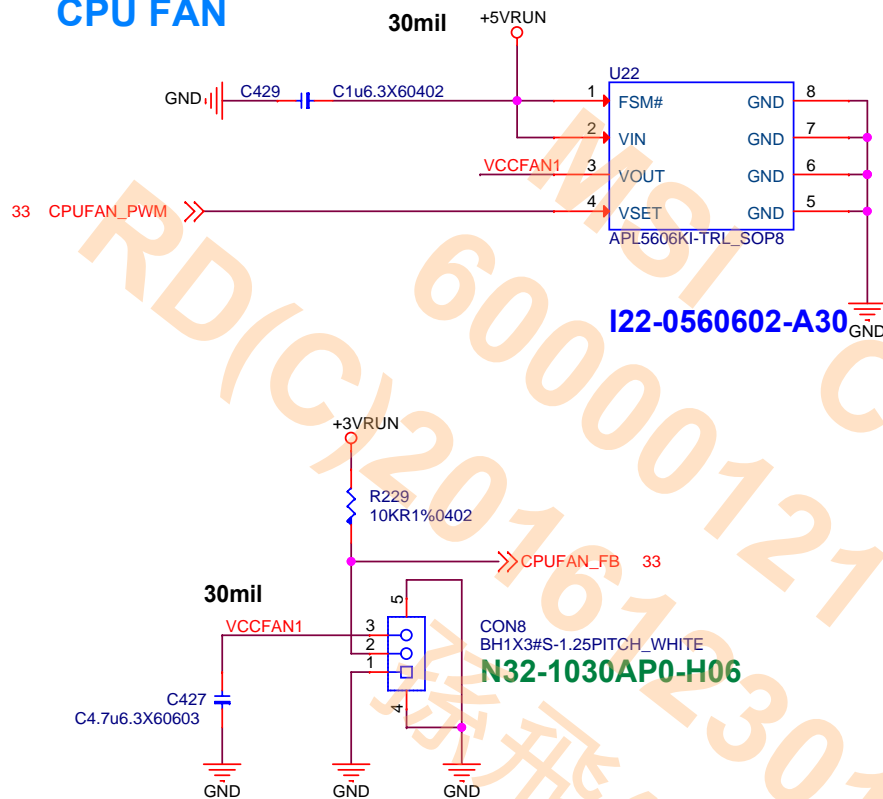
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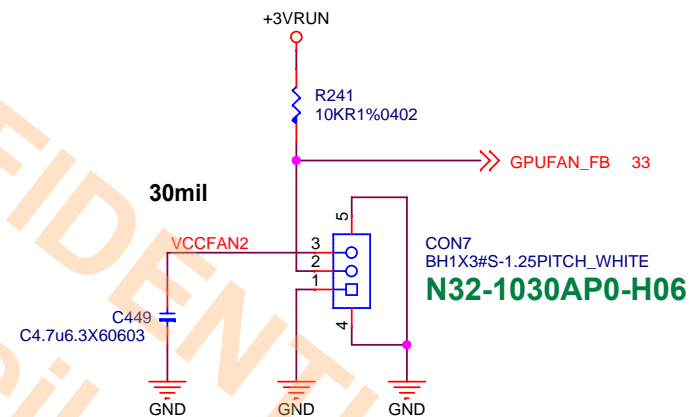
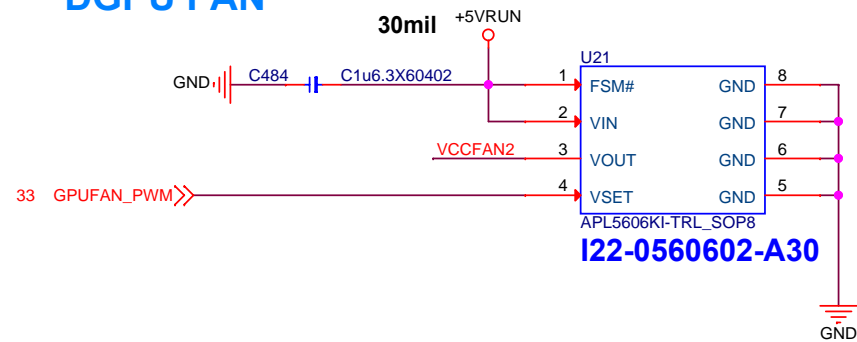
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CPU FAN



DGPU FAN



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

CPU FAN/DGPU FAN

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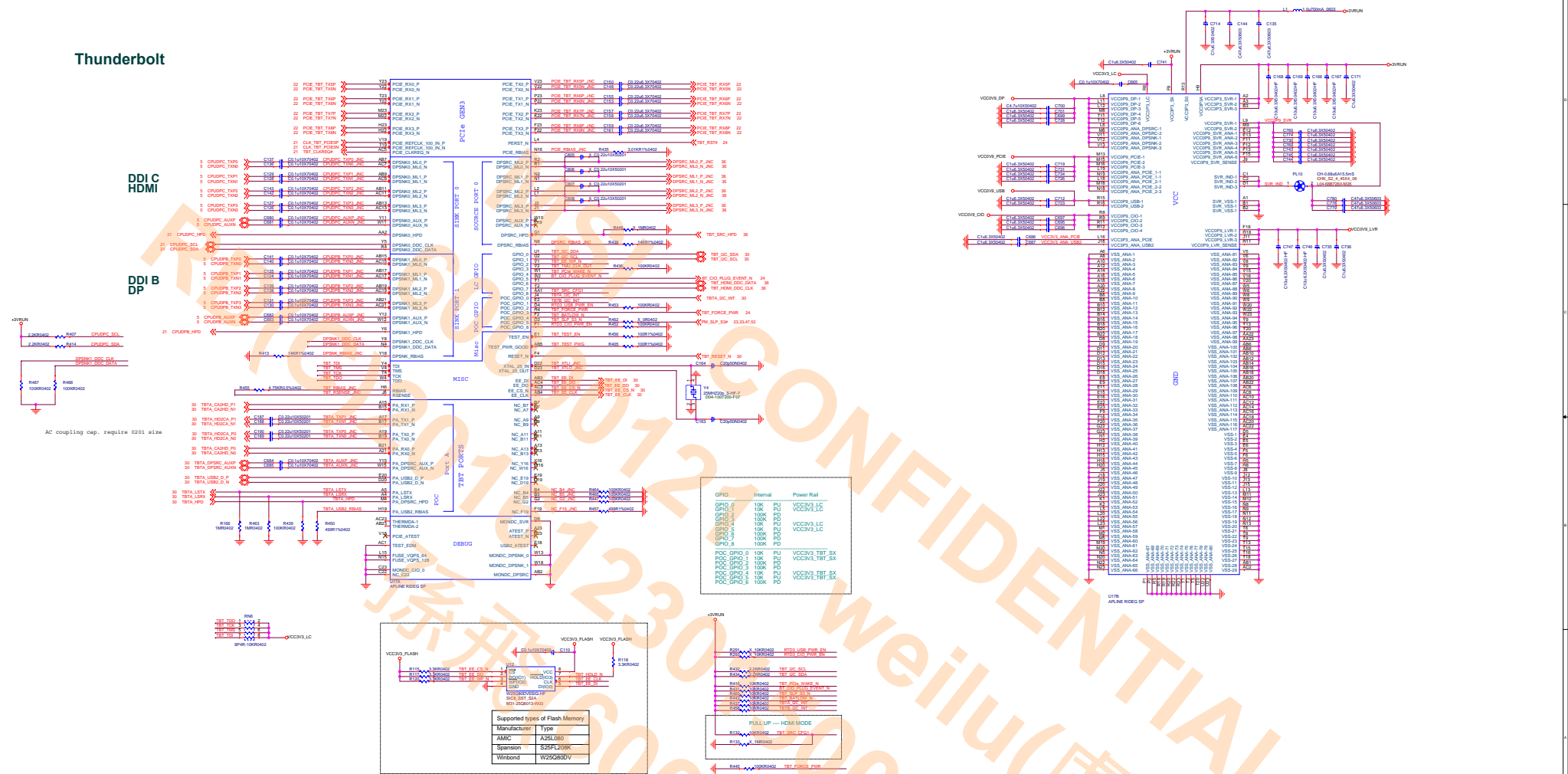
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Thunderbolt

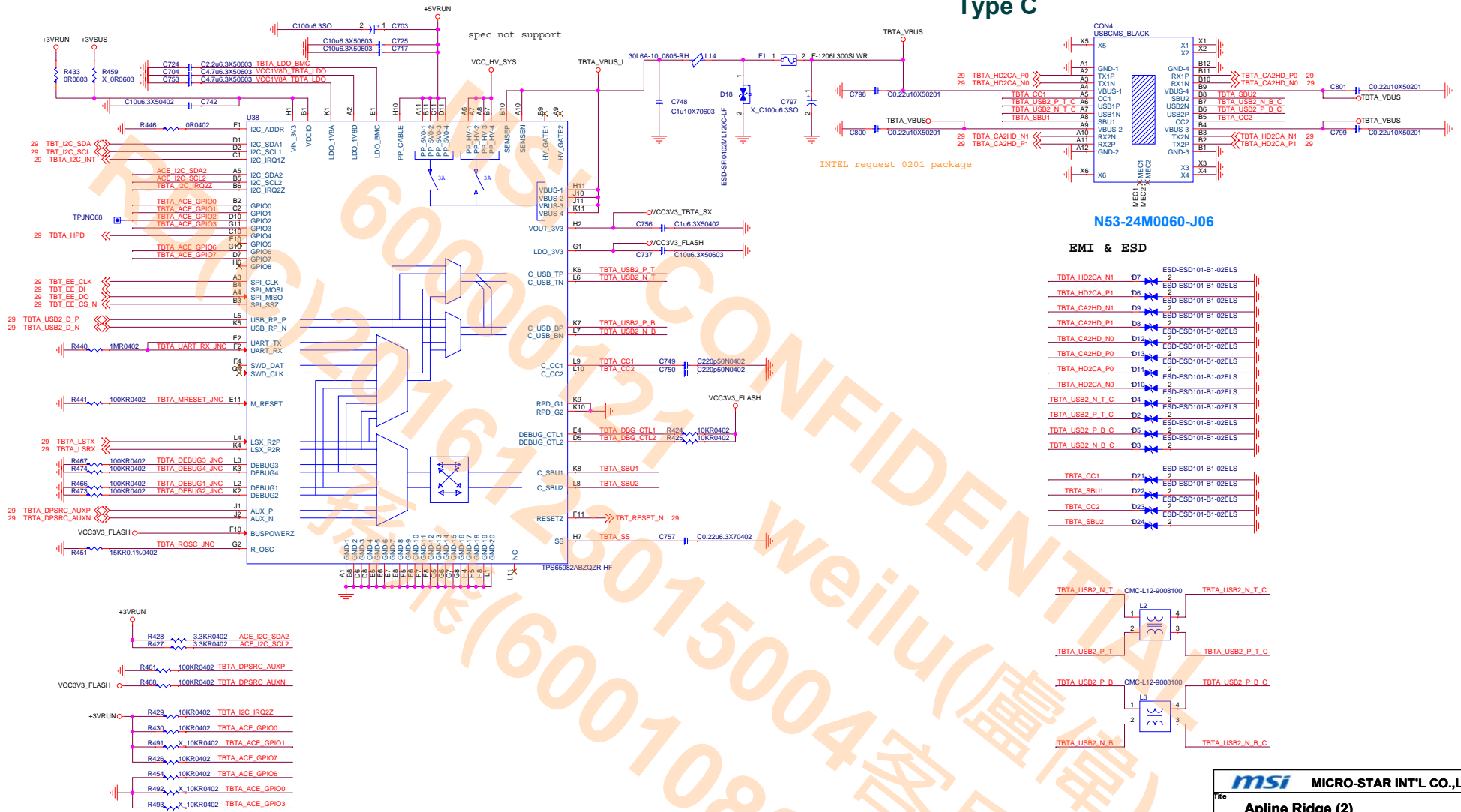
DDI C
HDMI

DDI B
DP

AC coupling cap. require 0201 size



Type C



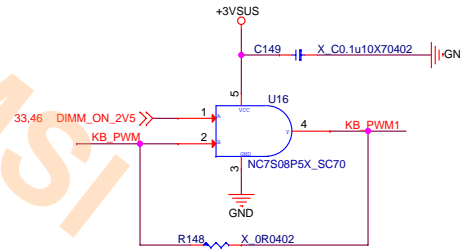
Backlight

Place Close eDP Connector
Reserve for EMI

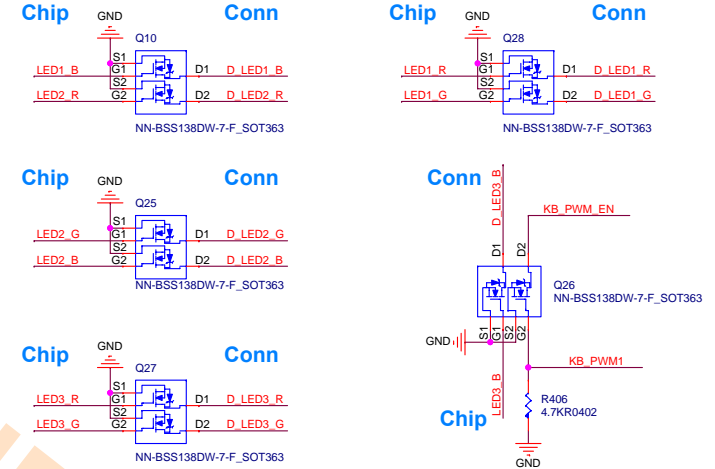
Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5-21V)
37	BL_PWR	Backlight power (5-21V)
38	BL_PWR	Backlight power (5-21V)
39	BL_PWR	Backlight power (5-21V)
40	HSYNC	HSYNC output from Tcon

LED Driver IC(EPF021J)

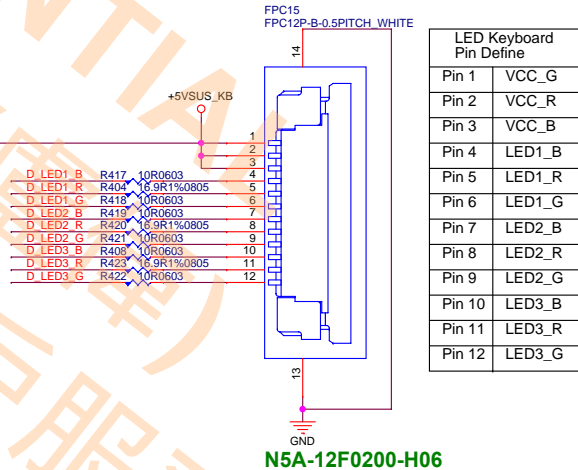
LED KB FLASH ERROR



EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

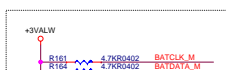
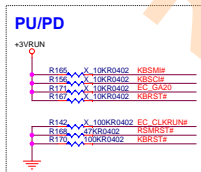
N5A-12F0200-H06

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Title	LED Driver IC
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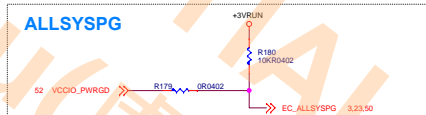
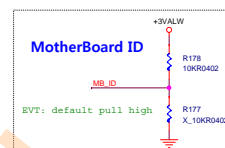
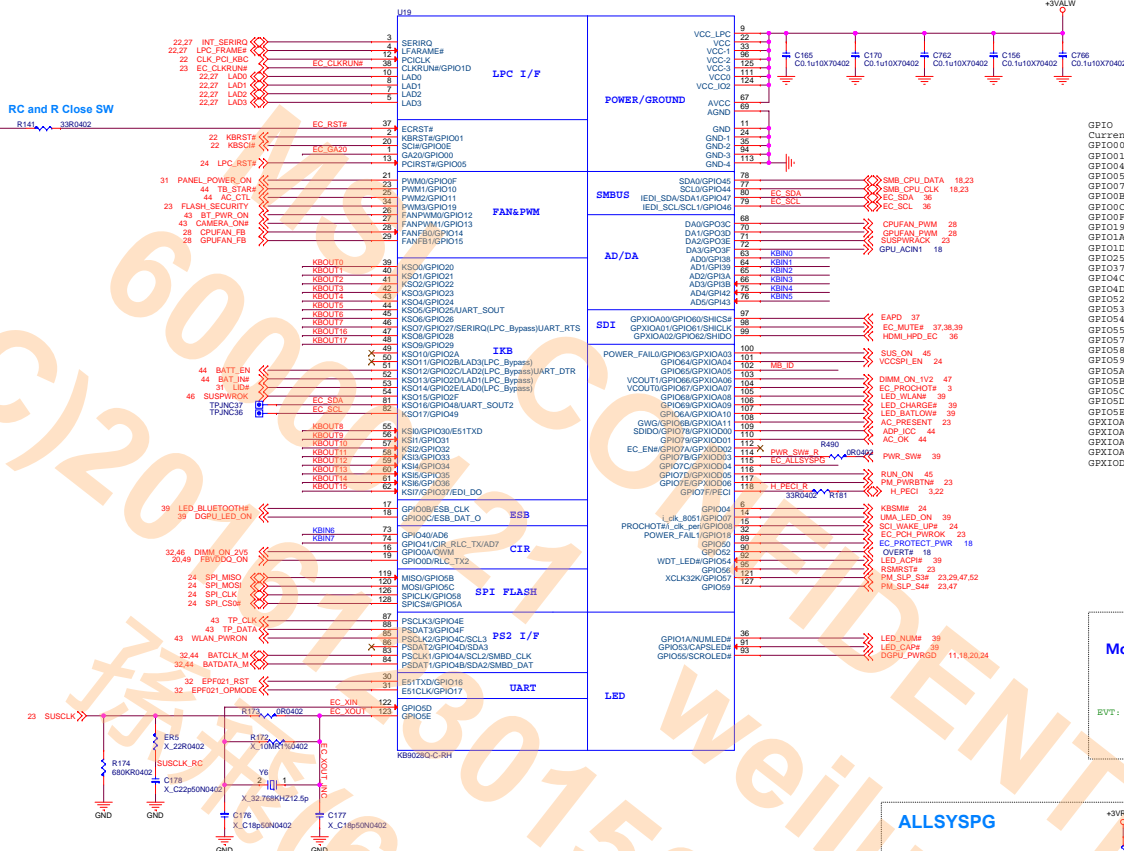
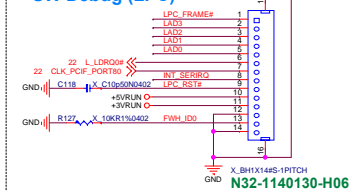
B07-F021J14-EB3

Pin12 & Pin13 have diff branch

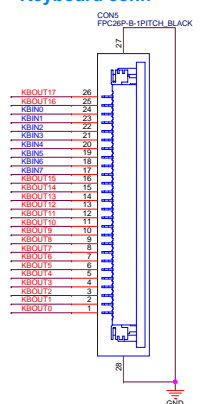
Hardware Reset



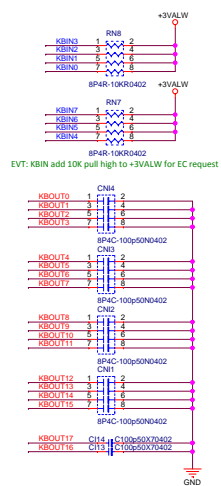
SW Debug (LPC)



Keyboard conn



N5A-26F0340-H06



CardReader (RTS5250)

RTS5250 Colay RTS5249

Power Trace

Pin11(3V3_IN) / Pin 12(CARD_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD_VDD2)trace fixed width is 30 mils (minimum)

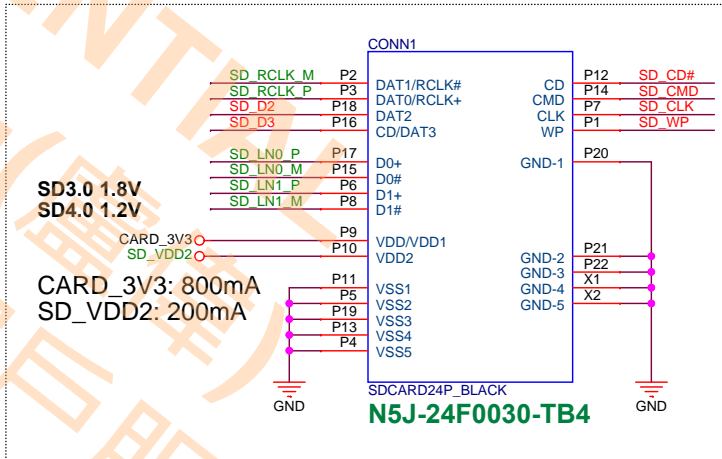
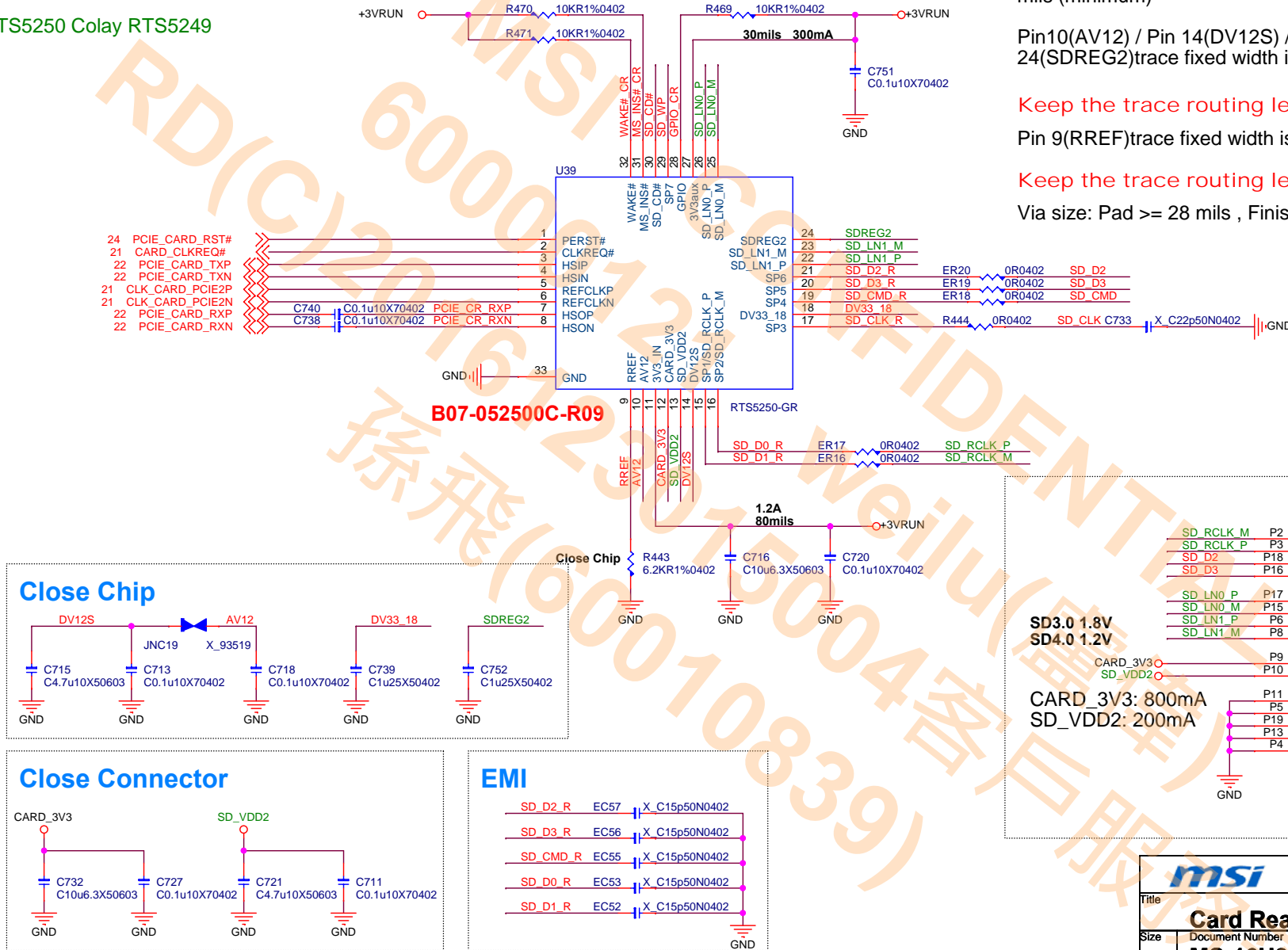
Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33_18) / Pin 24(SDREG2)trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Pin 9(RREF)trace fixed width is 12 mils (minimum)

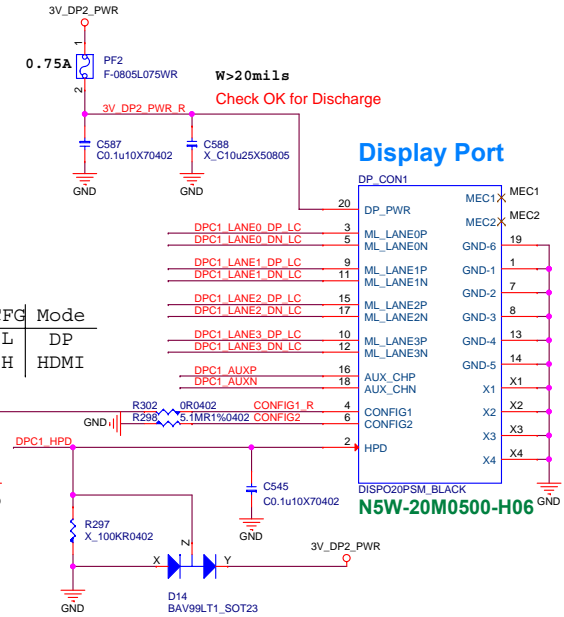
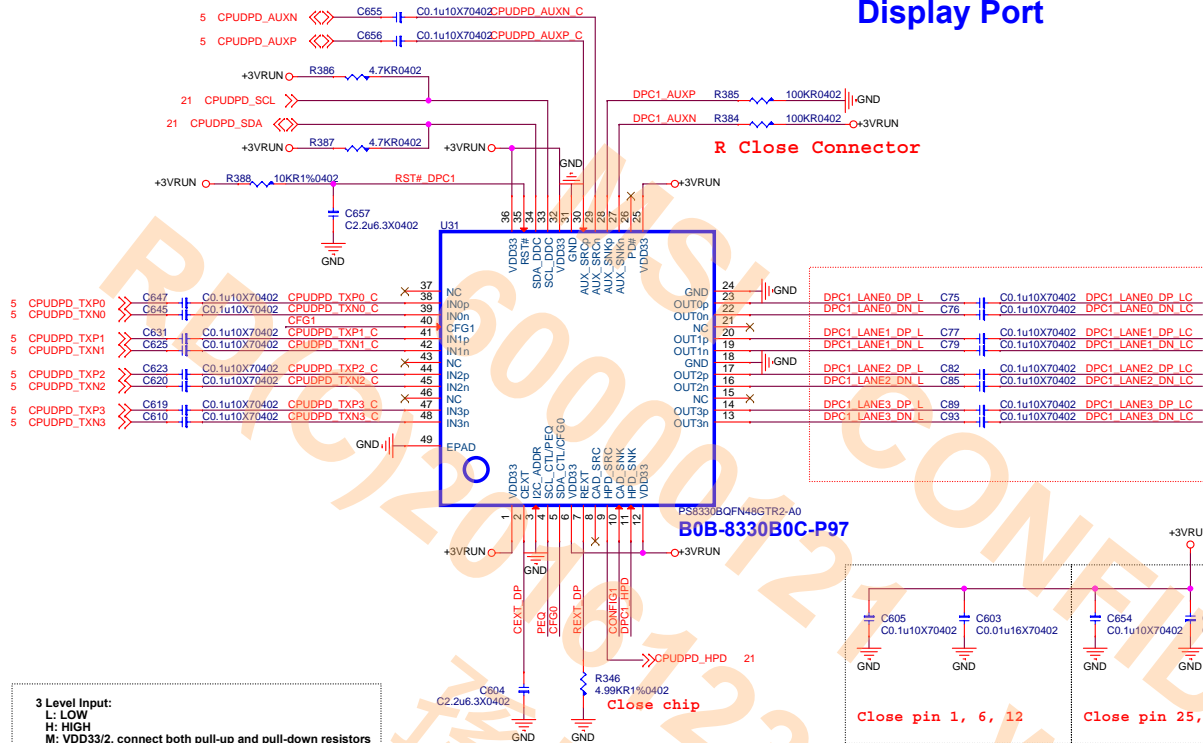
Keep the trace routing lengths is limit to 200 mils

Via size: Pad >= 28 mils , Finished hole >= 16 mils.

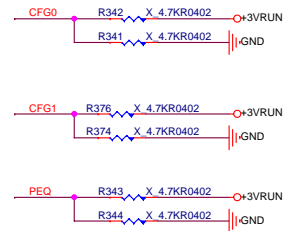


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Display Port



CAD_SNK Have internal Pull down 1Mohm.
 HPD_SNK Have internal Pull down 150kohm.
 No problem with Leakage from DP device
 The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

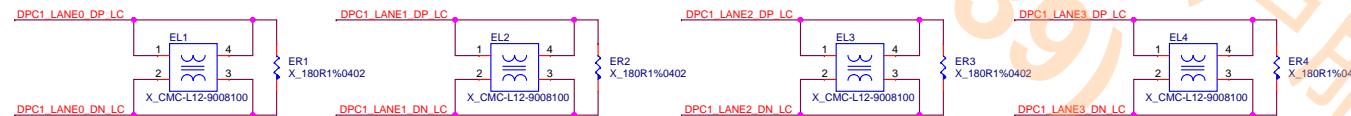


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
 L: default, automatic EQ enable & AUX interception enable
 H: automatic EQ disable & AUX interception enable
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

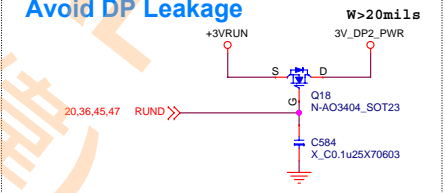
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
 H: default, auto test disable & input offset cancellation enable
 L: auto test enable & input offset cancellation enable
 M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150K Ohm, 3.3V I/O.
 L: default, LBQ, compensate channel loss up to 12dB @ HBR2
 H: HBQ, compensate channel loss up to 15dB @ HBR2
 M: LLBQ, compensate channel loss up to 5dB @ HBR2

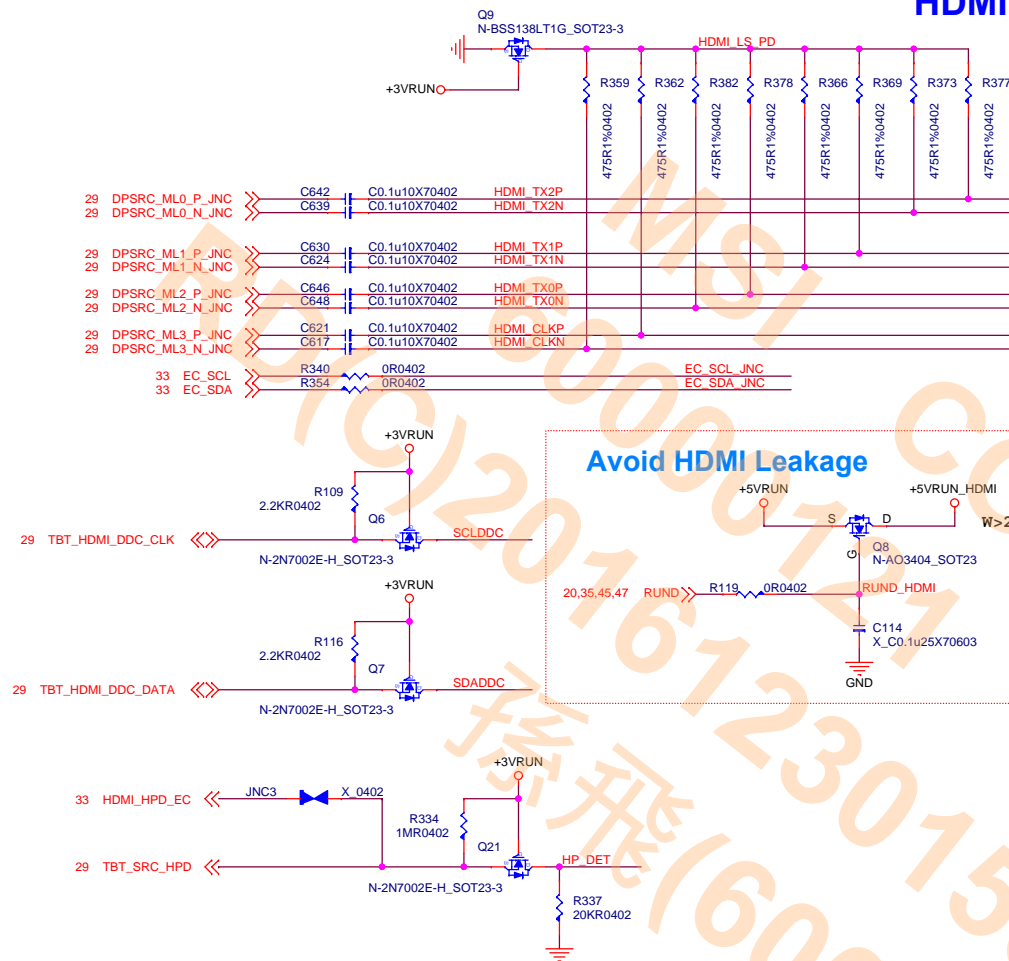
EMI Close Connector



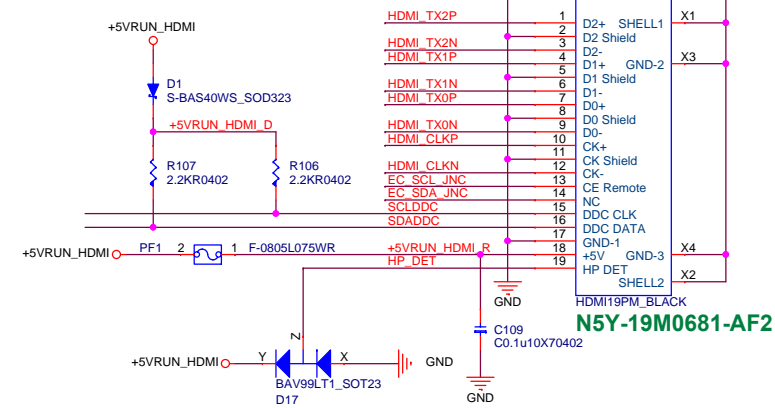
Avoid DP Leakage



HDMI Repeater

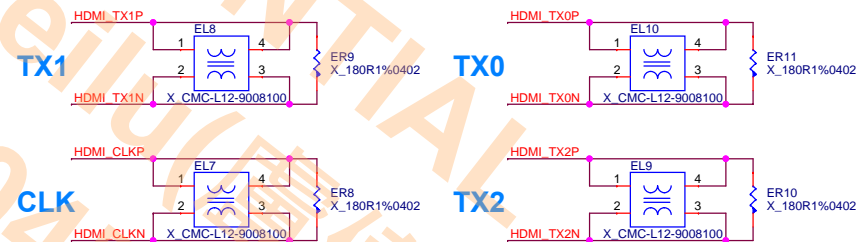


HDMI Connector



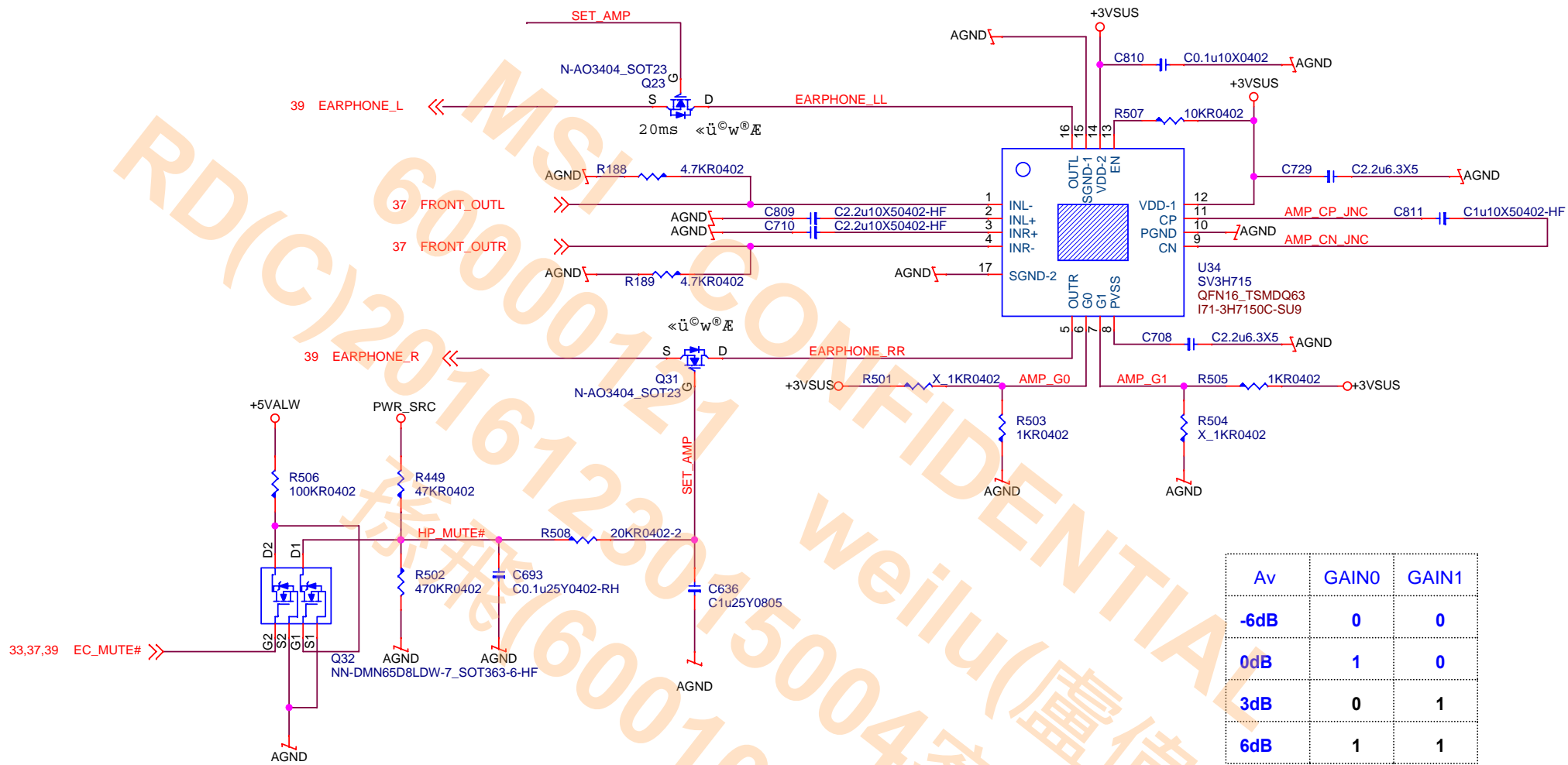
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

EMI Close Connector



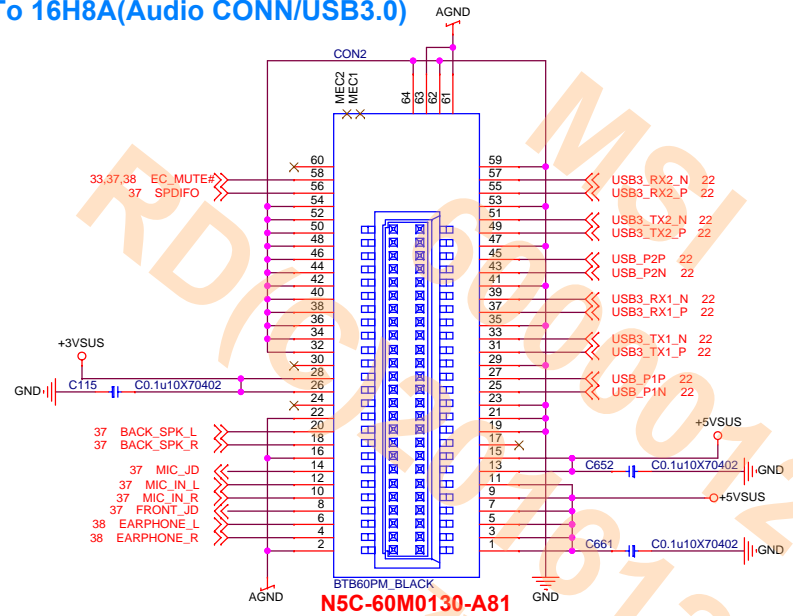
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Title		
HDMI Repeater		
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Headphone AMP

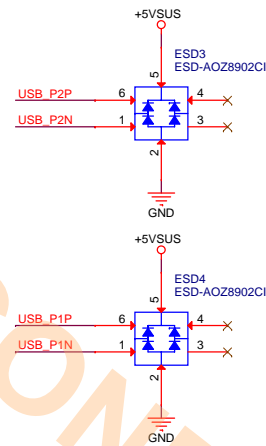


BTB CONN

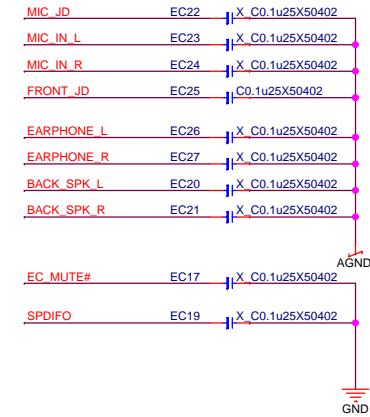
To 16H8A(Audio CONN/USB3.0)



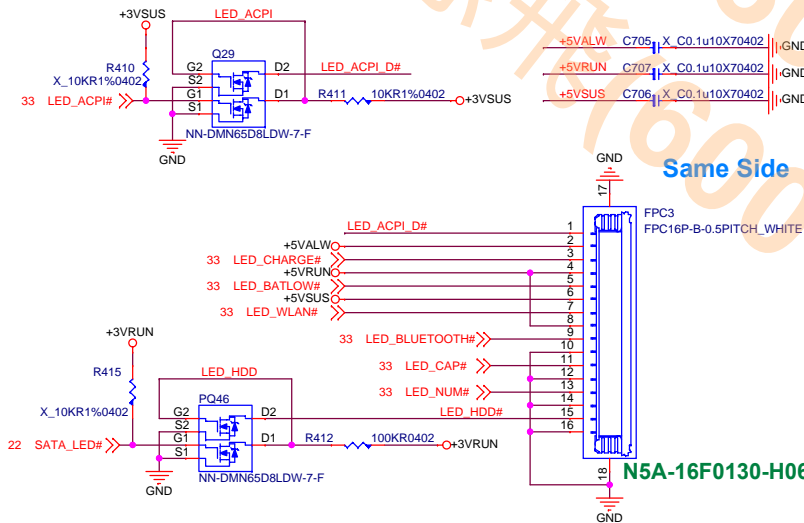
ESD



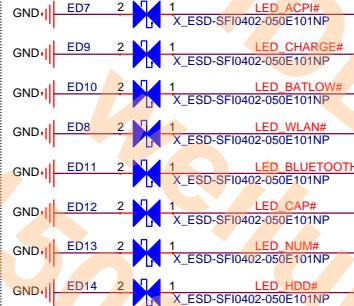
EMI



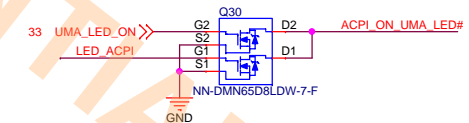
To 16H8B(LED Board)



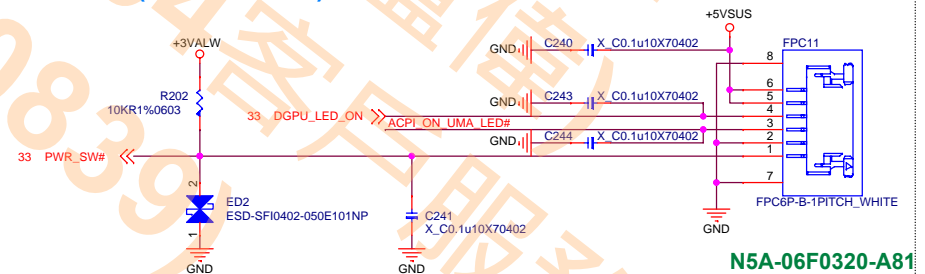
EMI



S3 Breath S0 No active



To 16H8C (Power Board)

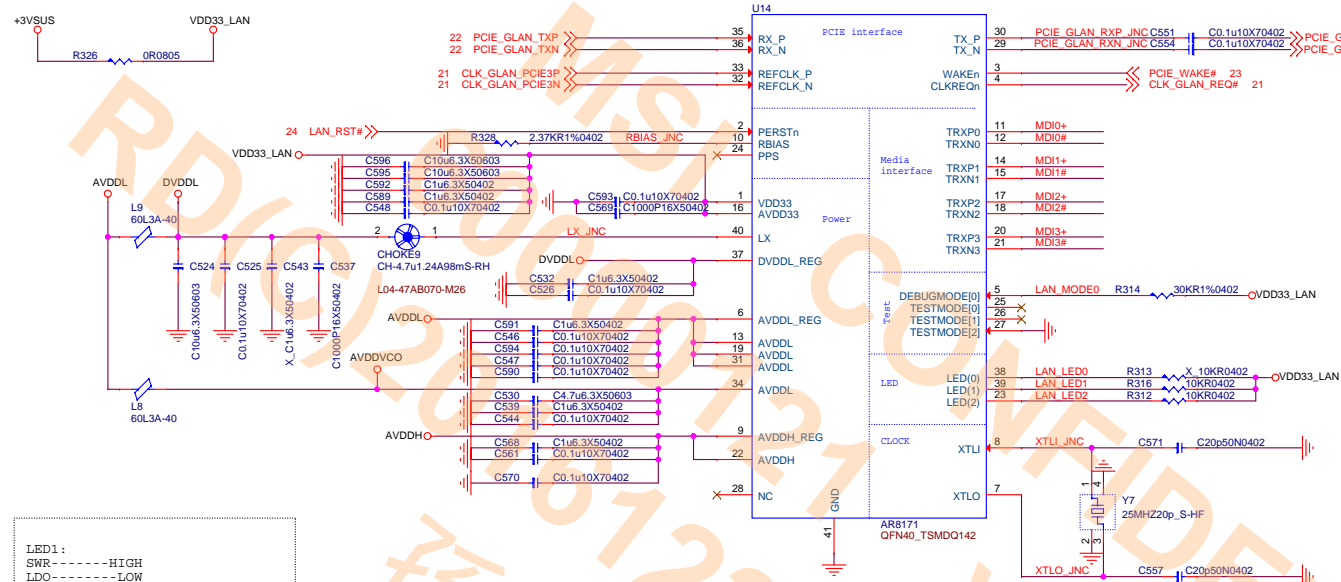


msi

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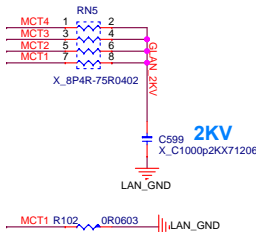
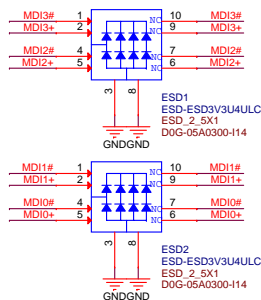
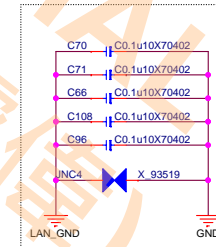
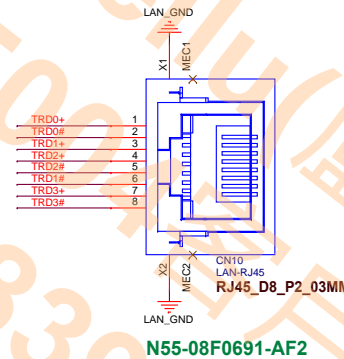
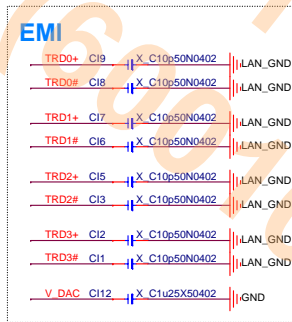
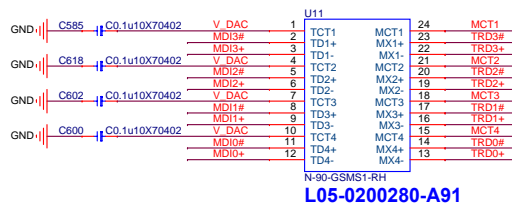
GIGA LAN(AR8171)



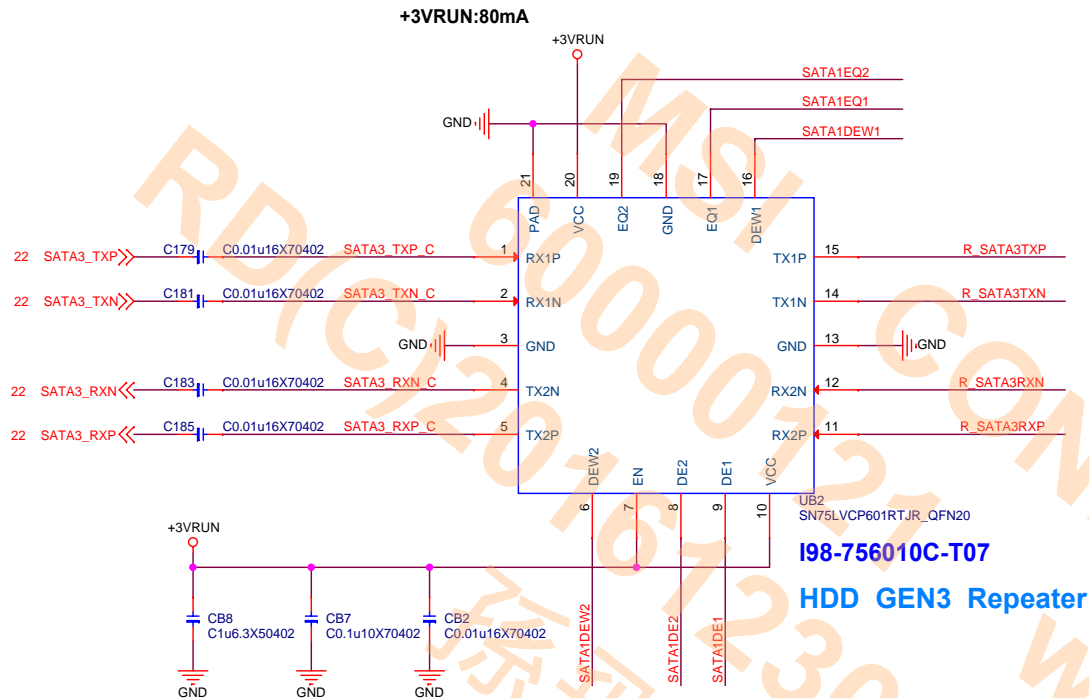
LED1:
SWR-----HIGH
LDO-----LOW
The chip have internal pull-up

LED2:
25MHz-----HIGH
48MHz-----LOW
The chip have internal pull-up

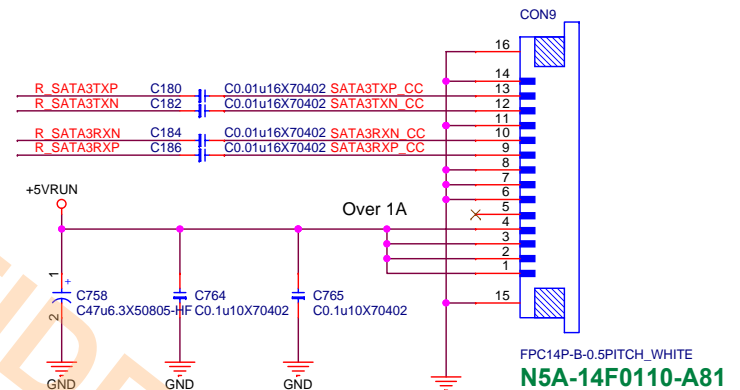
PIN 38 (LAN_LED0)	
AR8161/71	NC
E2400	Stuff



HDD (With Repeater)



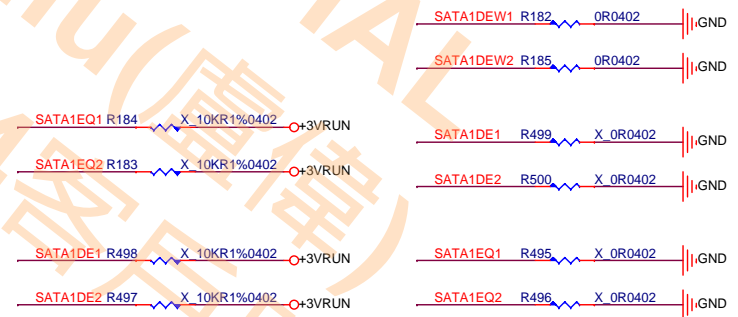
BTB Connector



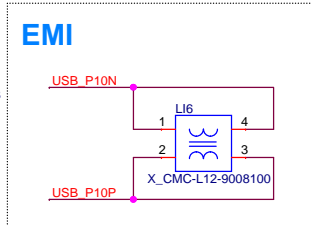
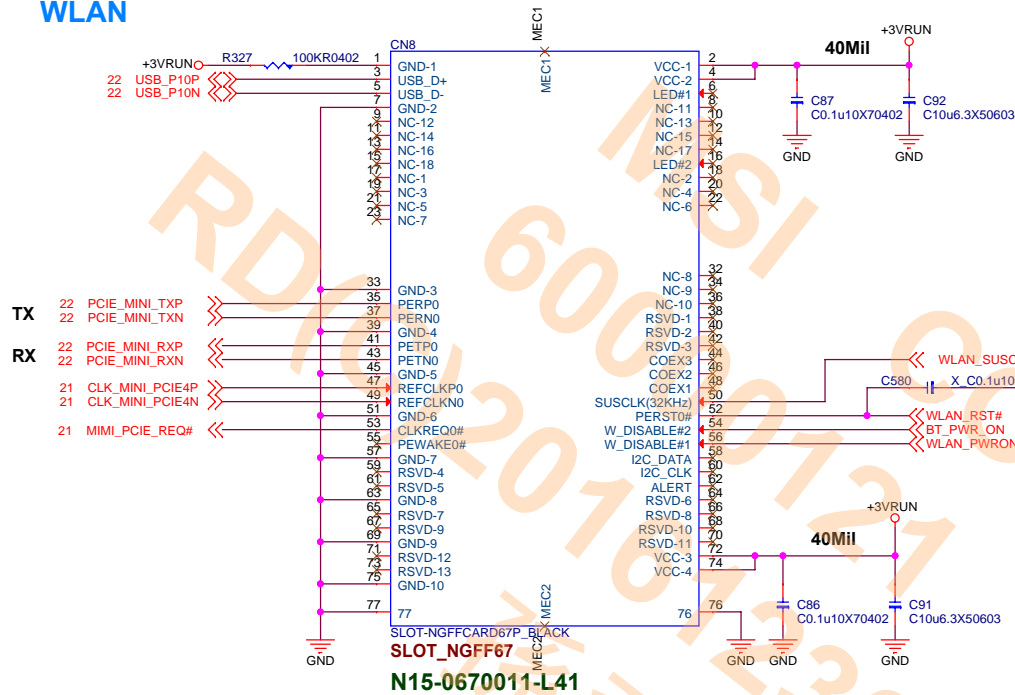
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis Pulse duration, long (recommended setting when link operates at SATA 1.5/3/6 Gbps)

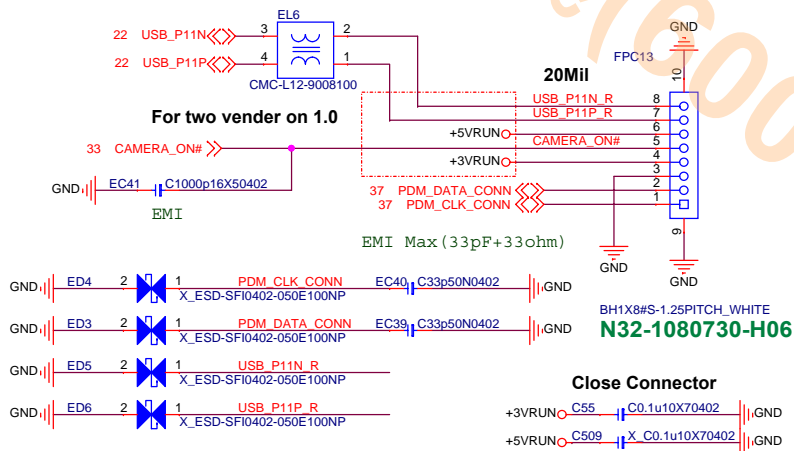


WLAN

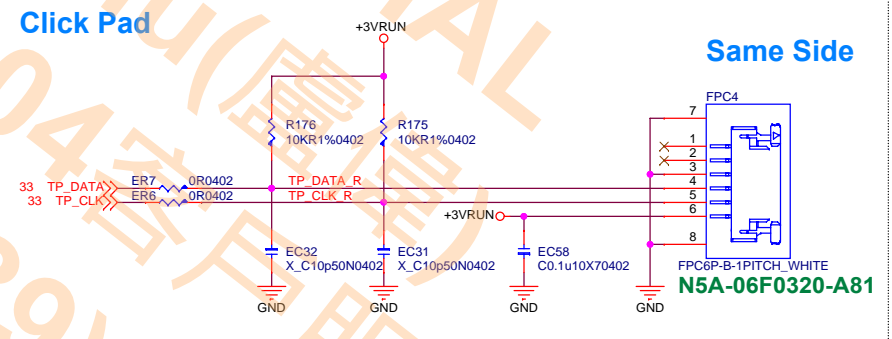


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

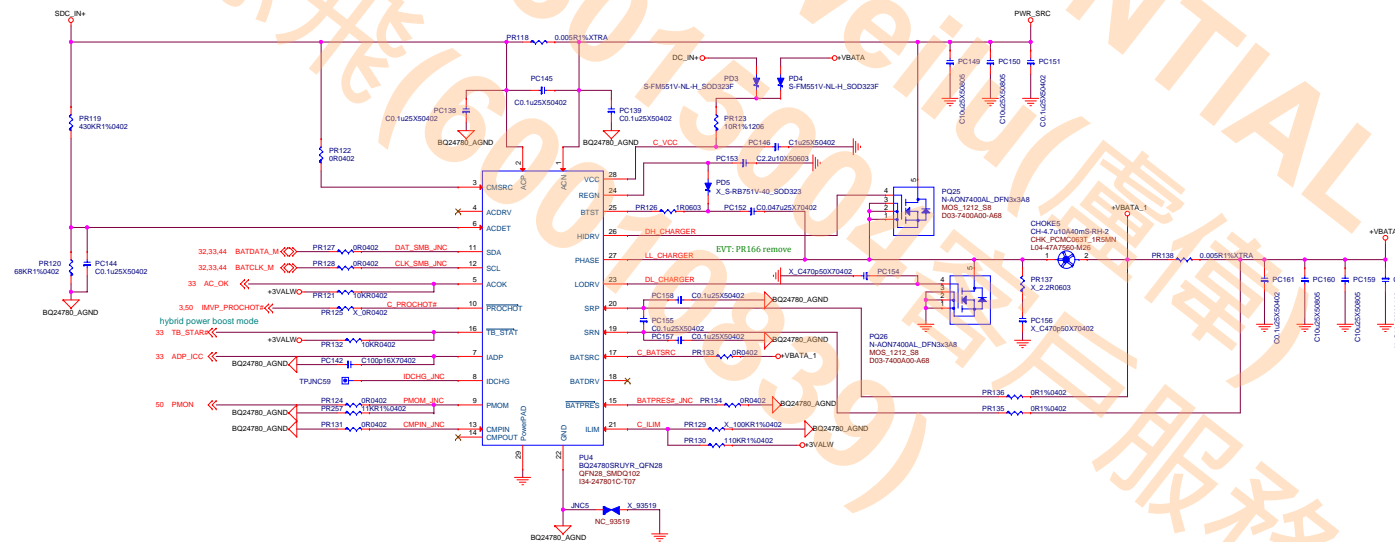
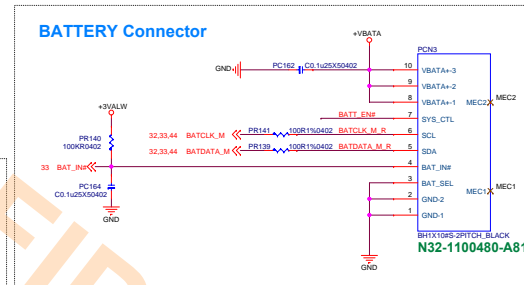
CAMERA



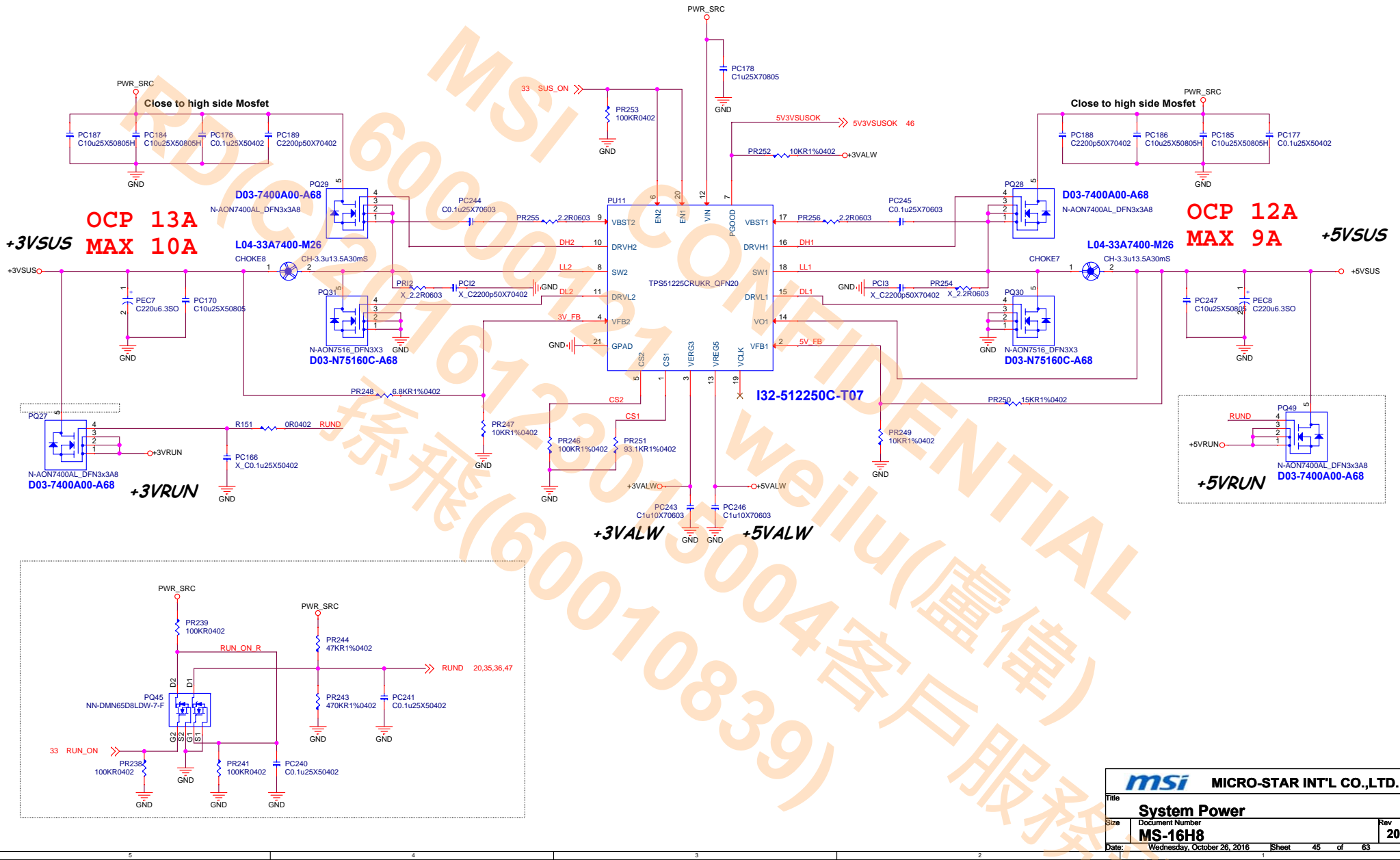
Click Pad



Battery Select

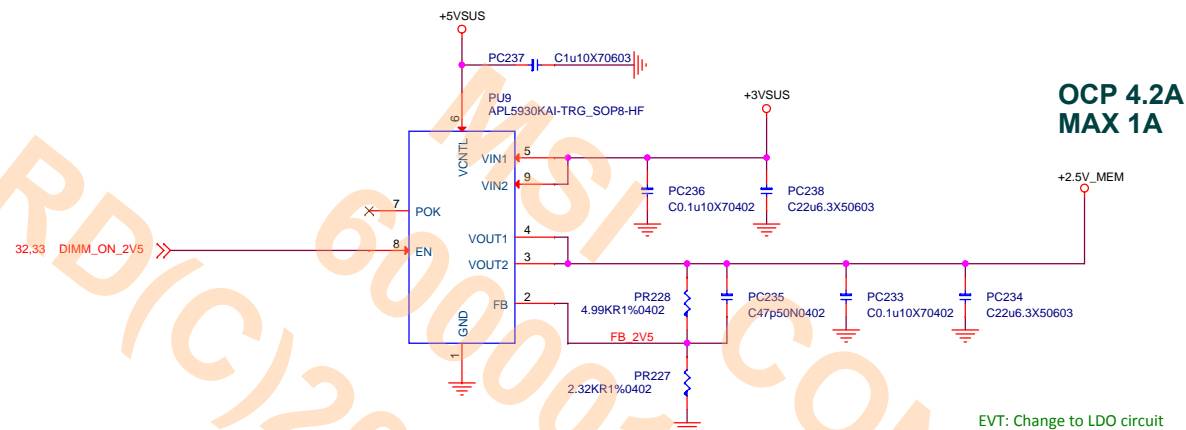


System Power

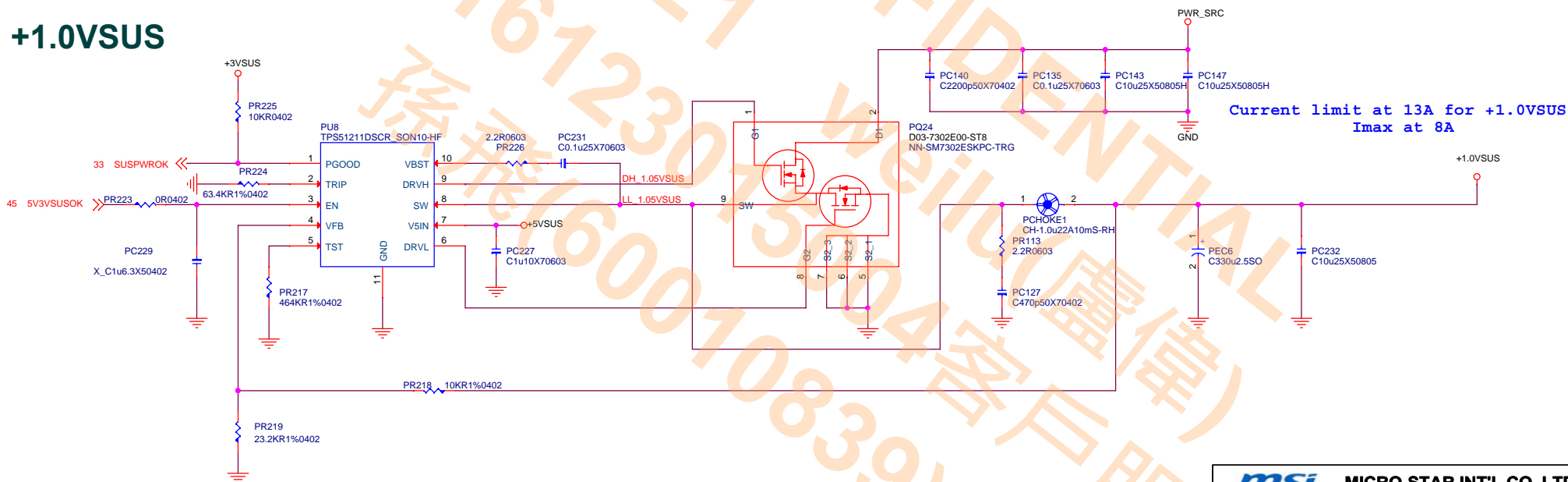



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+2.5V_MEM



+1.0VSUS



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DGPU POWER / UP1642PQAG

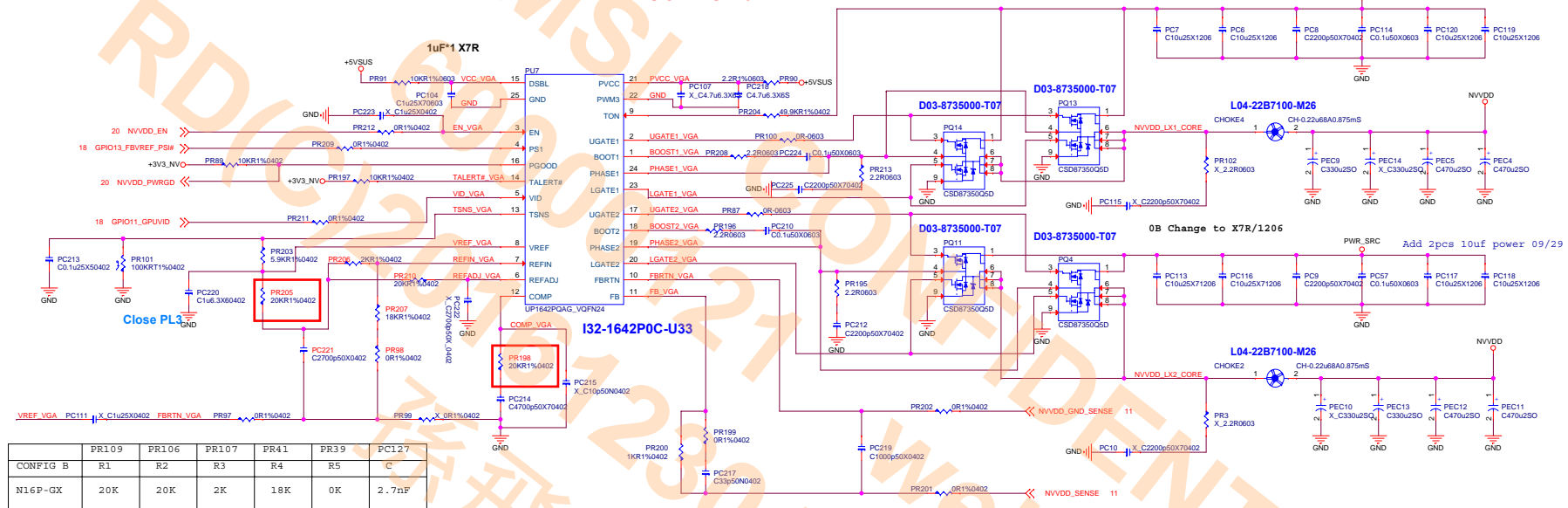
DGPU POWER NVVDD

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 87A
EDP-Con 51.1A

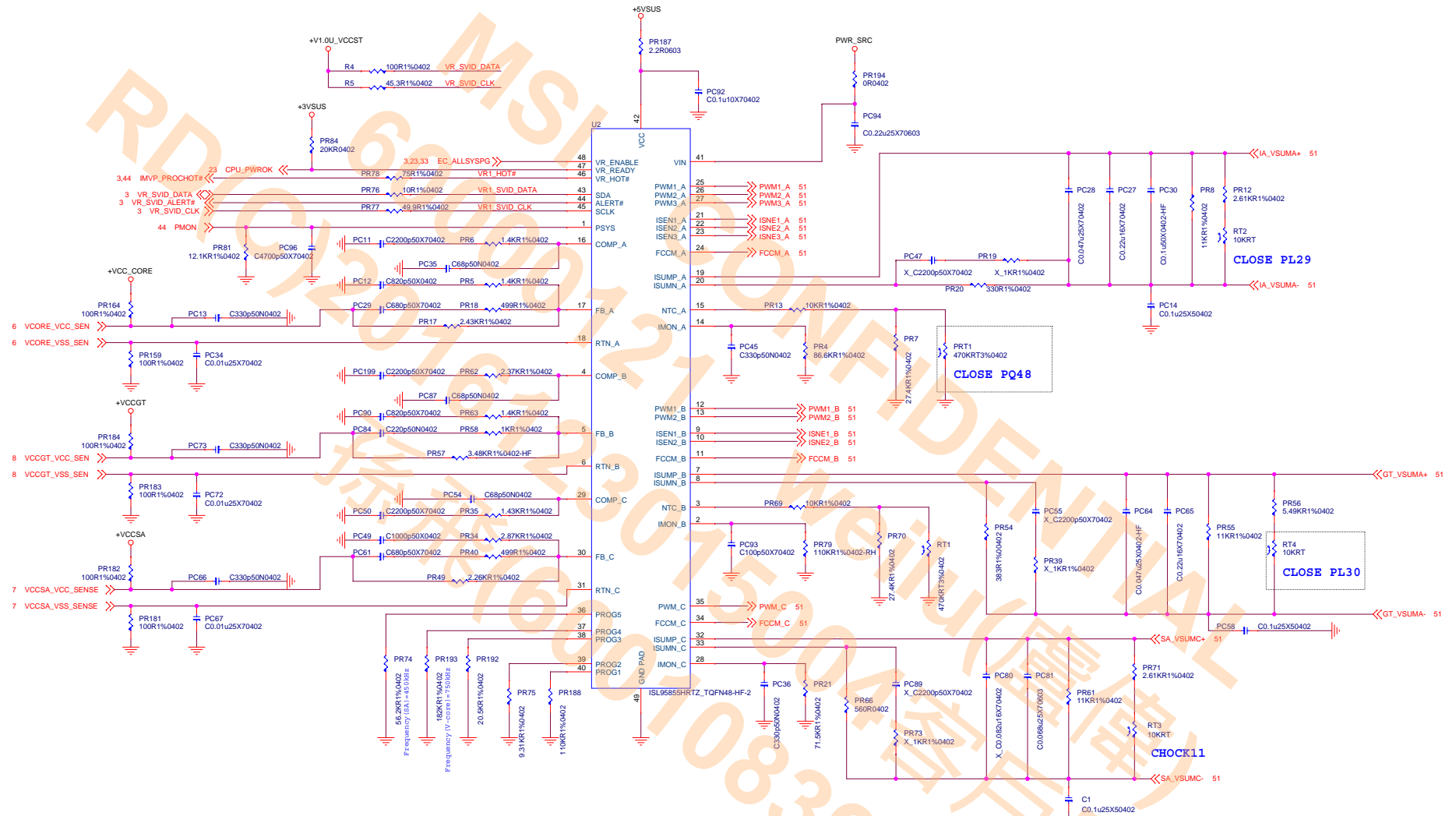
0B Change to X7R/1206
1.0 Change to X5R/1206 high

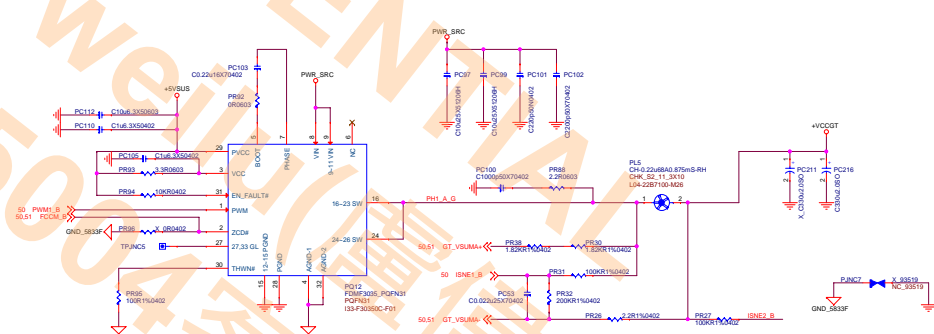
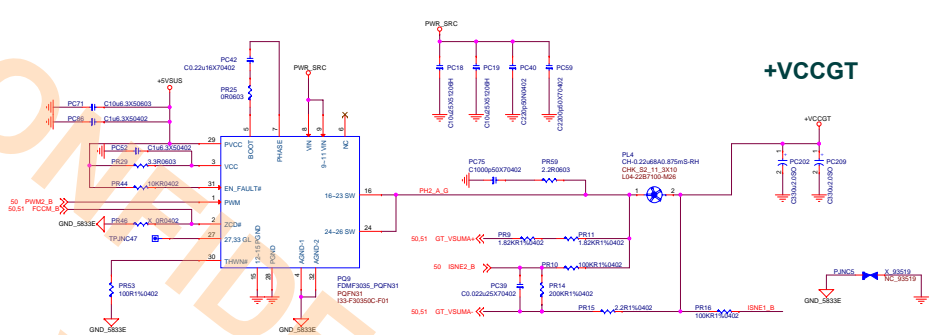
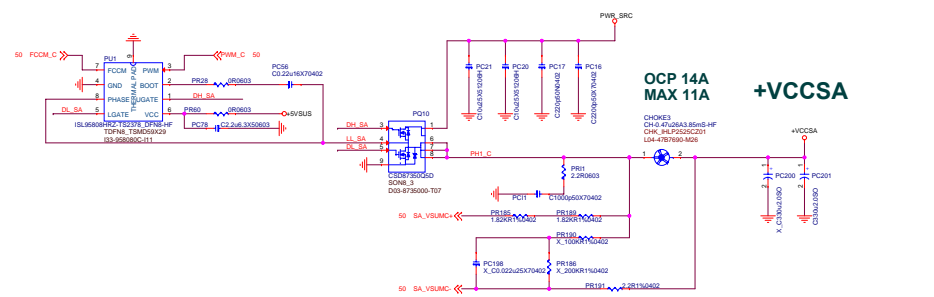
PWR_SRC Add 2pcs 10uf power 09/29

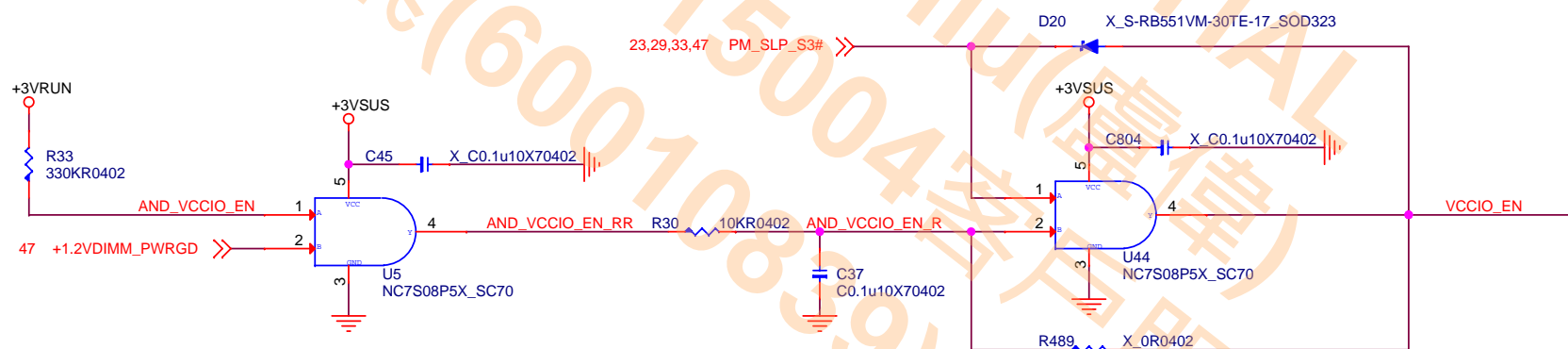
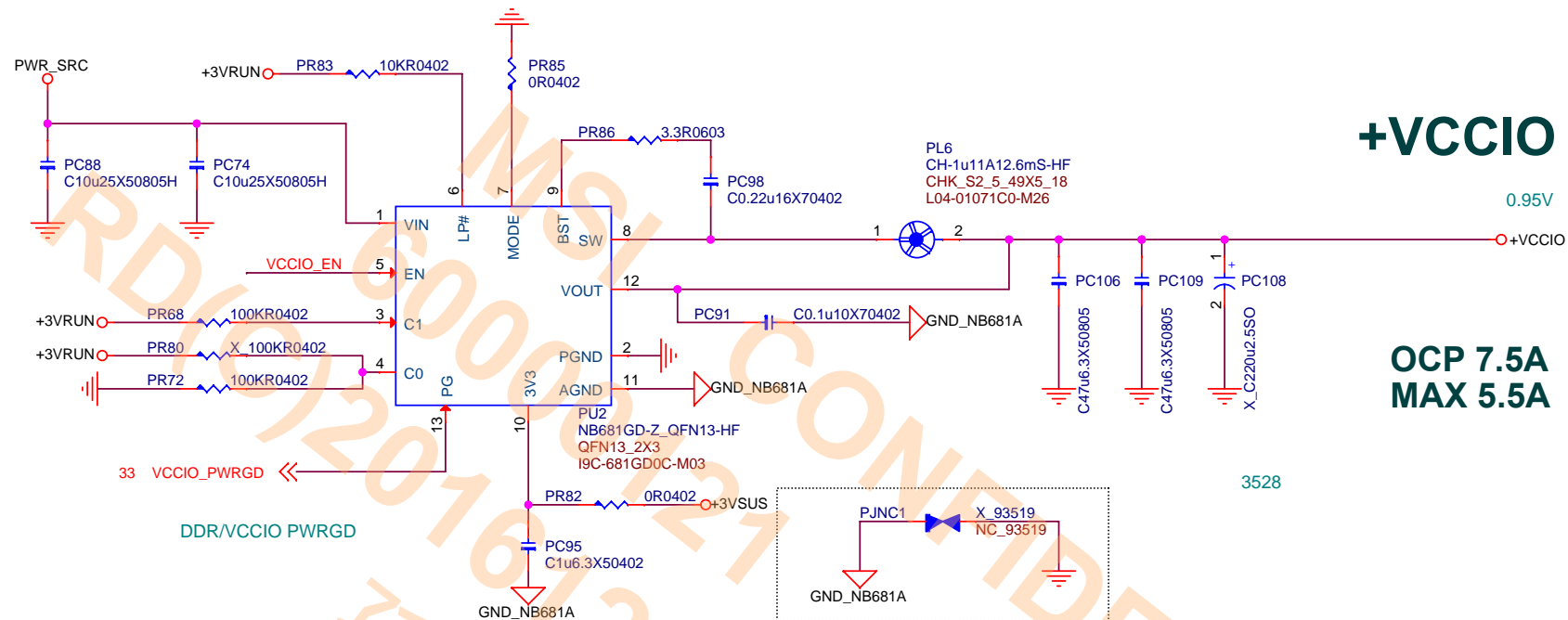


	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG B	R1	R2	R3	R4	R5	C
N16P-GX	20K	20K	2K	18K	0K	2.7nF

CPU Power IC (ISL95855)

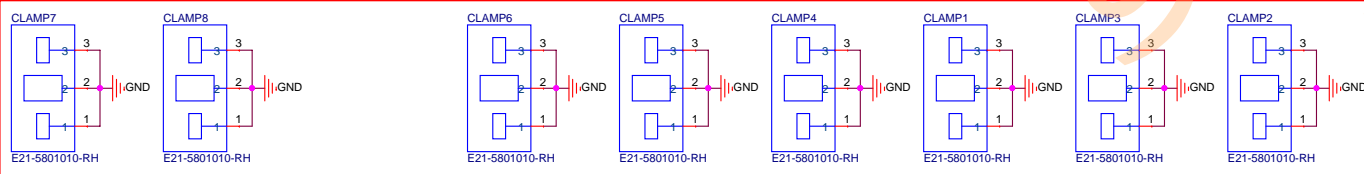
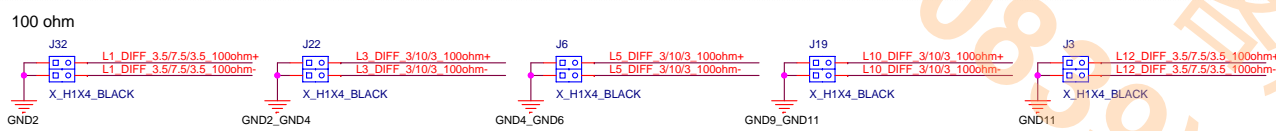
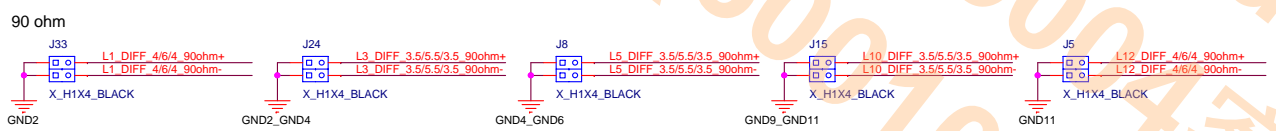
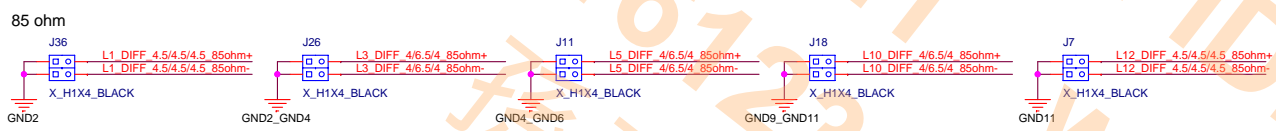
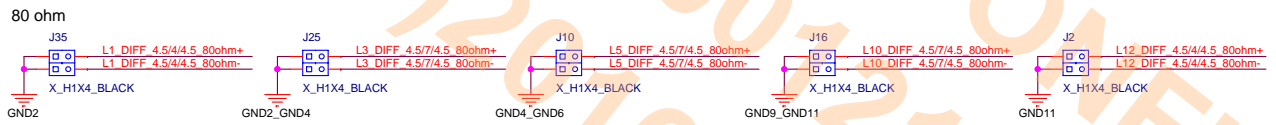
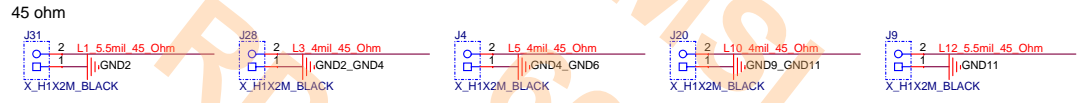




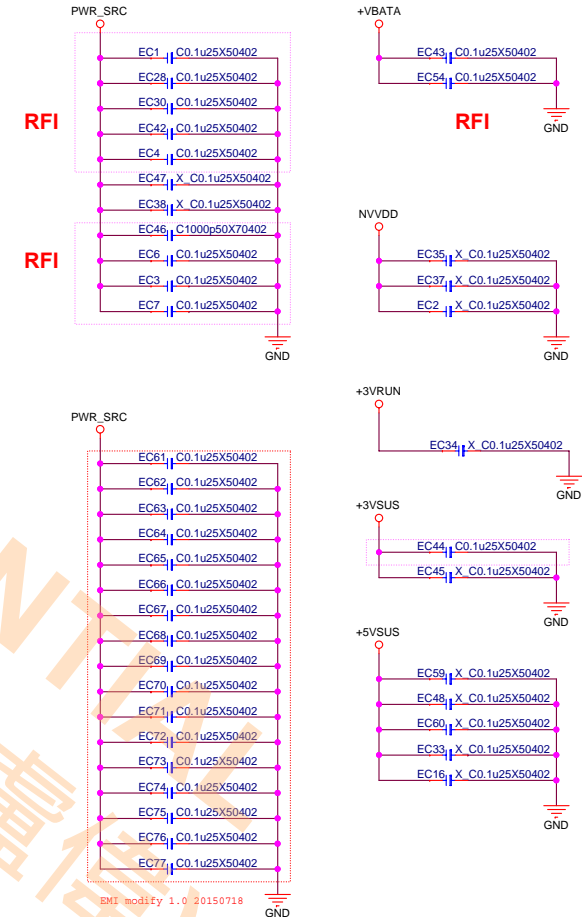


EMI/ Impedance

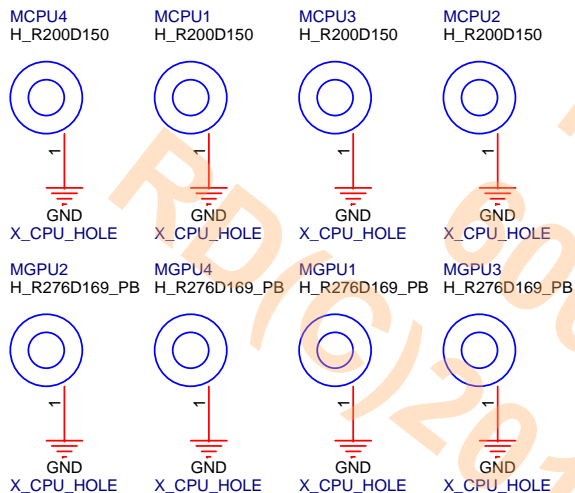
Impedance Connector No PN



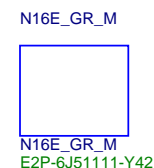
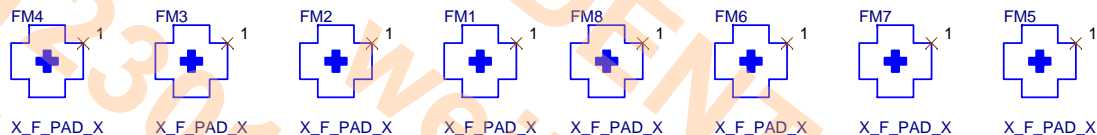
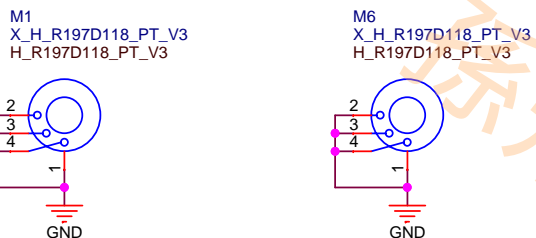
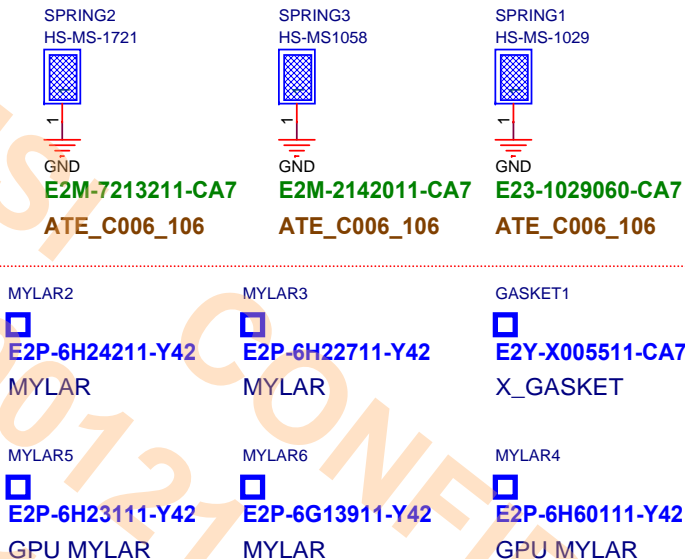
EMI



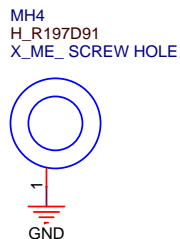
CPU/GPU Holes



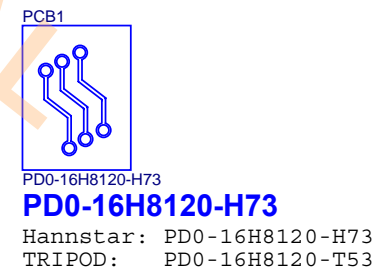
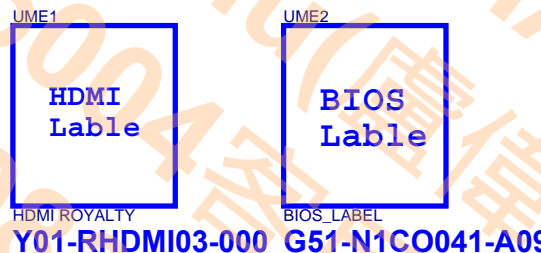
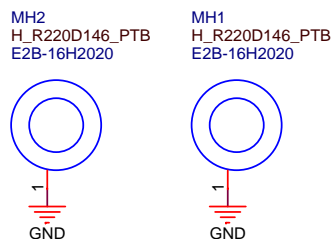
EMI



Fan Hole



SSD Stand off

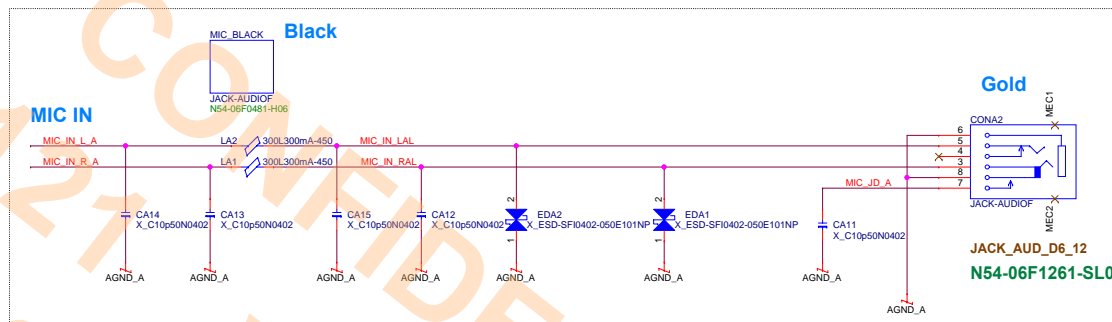
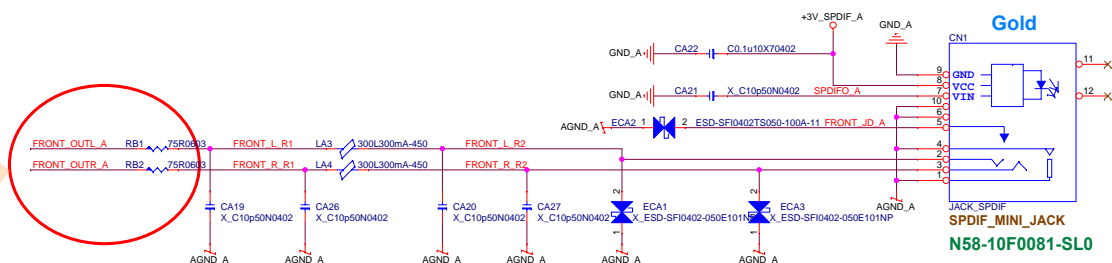
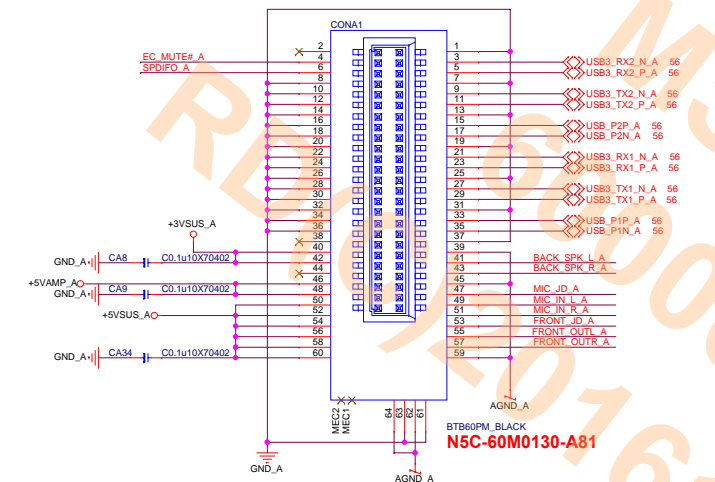


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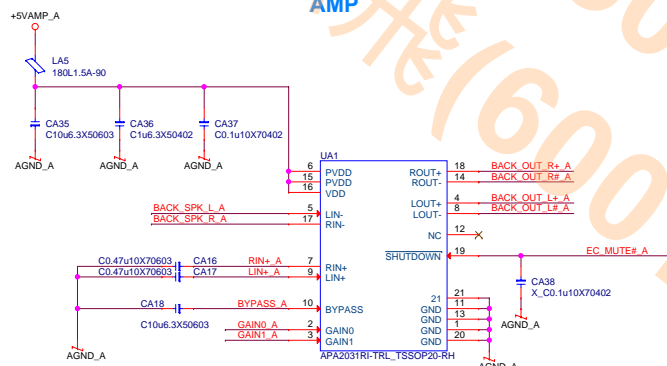
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Screw/ME		
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16H8A Board (Audio CONN)

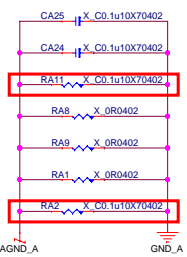
BTB Connector From MB CONN Pin Current Capability : 0.5A/Pin



AMP



EMI

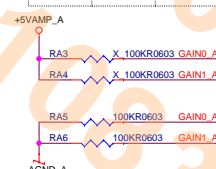


Change to Cap

Change to Cap

For APA2031

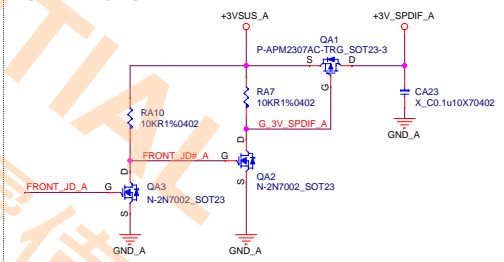
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



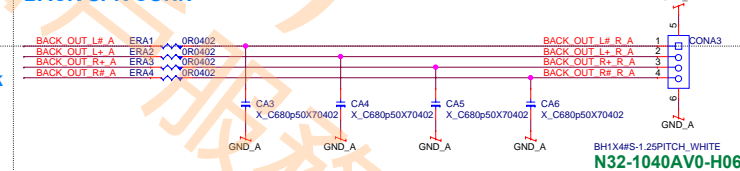
FRONT OUT



SPDIF Power



BACK SPK CONN



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[A] Audio

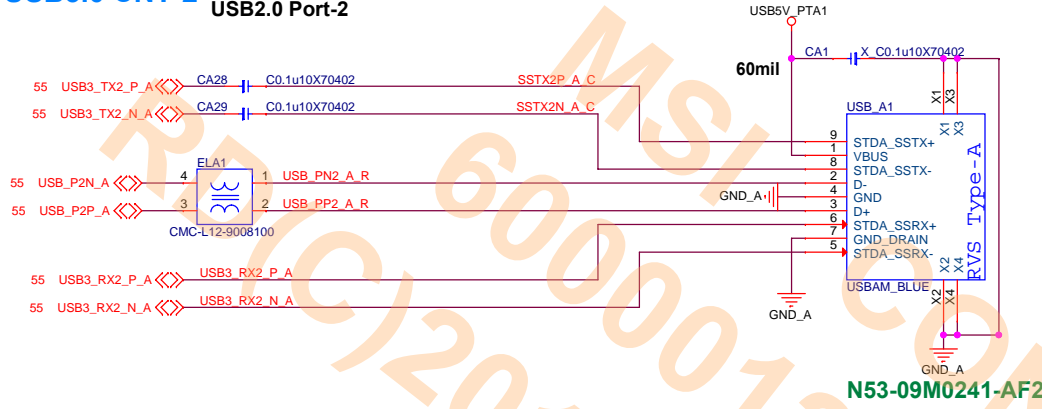
MS-16H8

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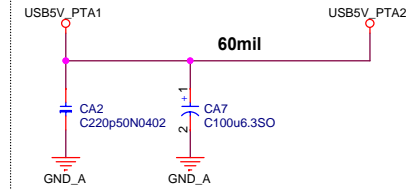
Rev 20

16H8C USB3.0 CNT-2/3

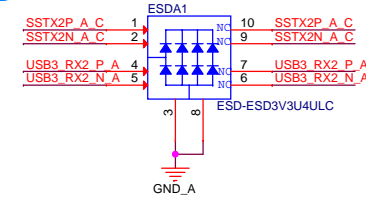
USB3.0 CNT-2 USB3.0 Port-2 USB2.0 Port-2



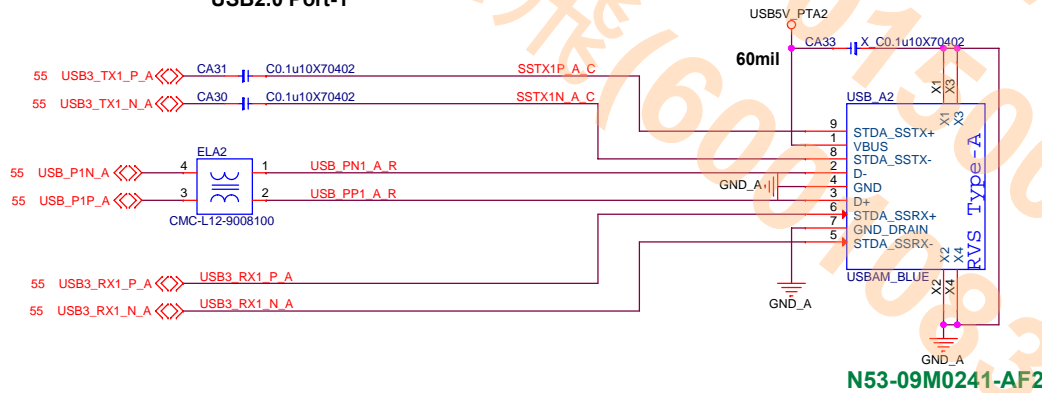
USB Power



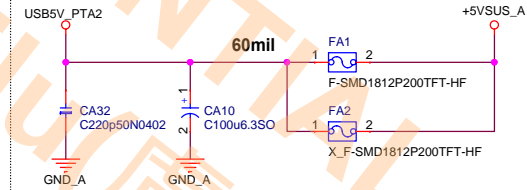
ESD



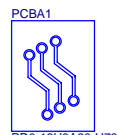
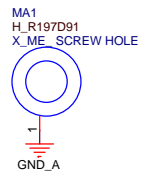
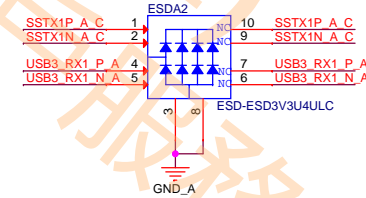
USB3.0 CNT-3 USB3.0 Port-1 USB2.0 Port-1



USB Power



ESD



PD0-16H8A20-H73
PD0-16H8A20-H73

Hannstar: PD0-16H8A20-H73
TRIPOD: PD0-16H8A20-T53

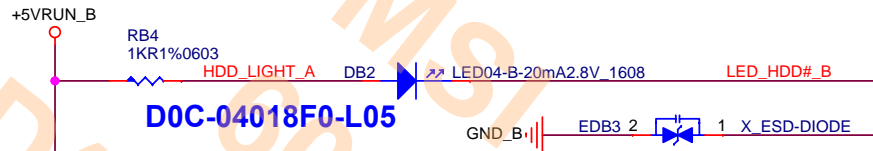
MYLARA1	MYLARA2
E2P-6H22812-G40	E2P-6H22311-G40
MYLAR	MYLAR

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Title [A] USB3.0 CNT-3/4	
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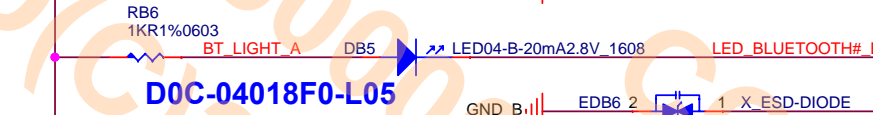
16H8B Board (LED Board)

LED

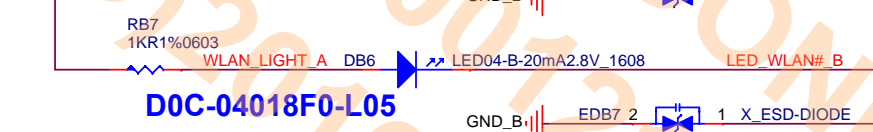
BLUE
(HDD)



BLUE
(BT)



BLUE
(WLAN)



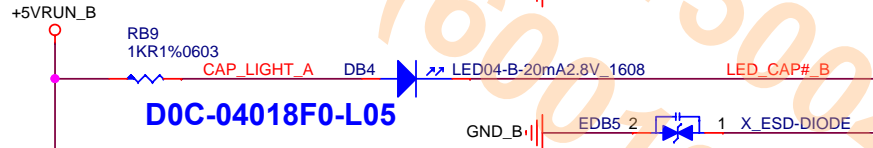
ORANGE
(BATLOW)



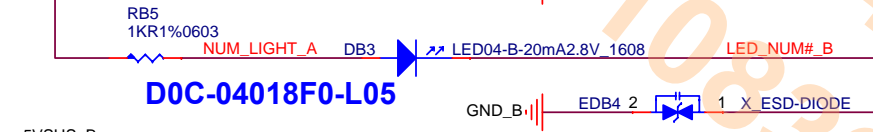
BLUE
(CHARGE)



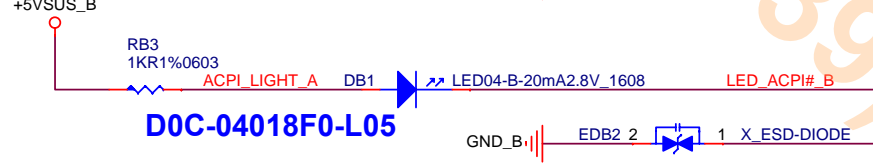
BLUE
(CAP)



BLUE
(NUM)



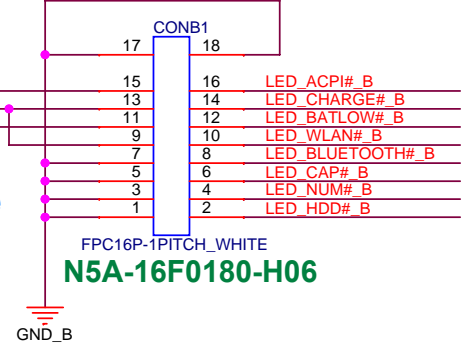
BLUE
(ACPI)



Connector

+5VALW_B
+5VRUN_B
+5VSUS_B

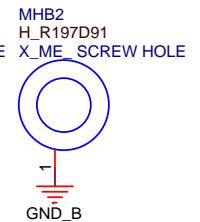
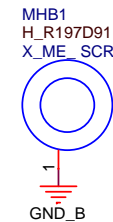
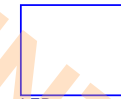
Same Side



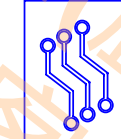
LED-R



LED



PCBB1

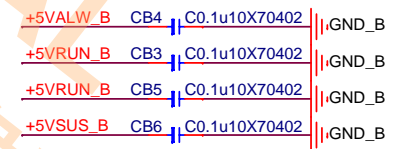


PD0-16H8B20-H73

PD0-16H8B20-H73

Hannstar: PD0-16H8B20-H73

TRIPOD: PD0-16H8B20-T53



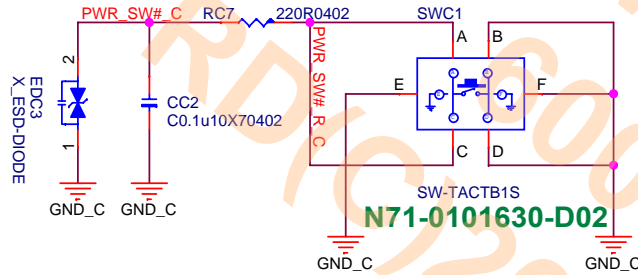
msi

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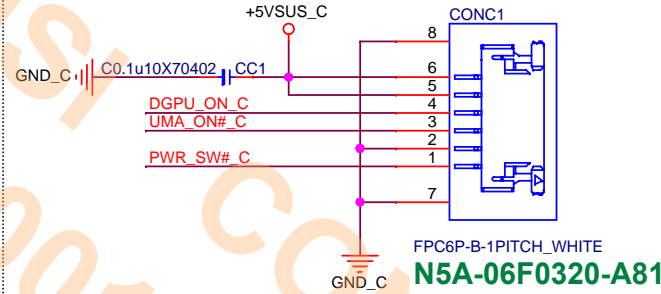
Title		
LED Board		
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16H8C Board (Power SW Board)

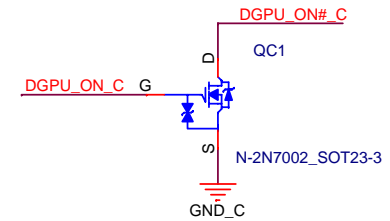
Power Switch



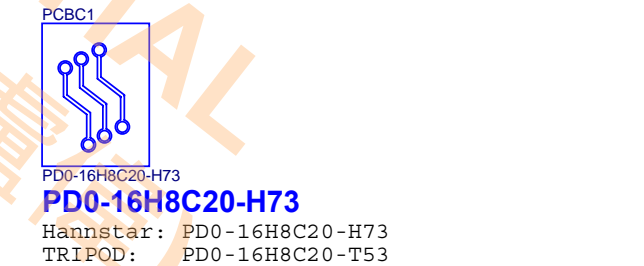
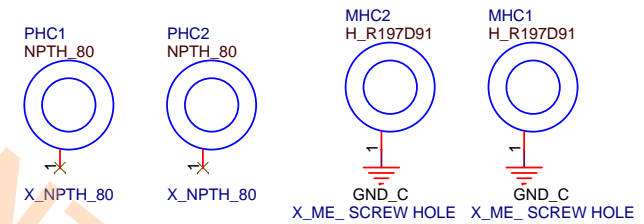
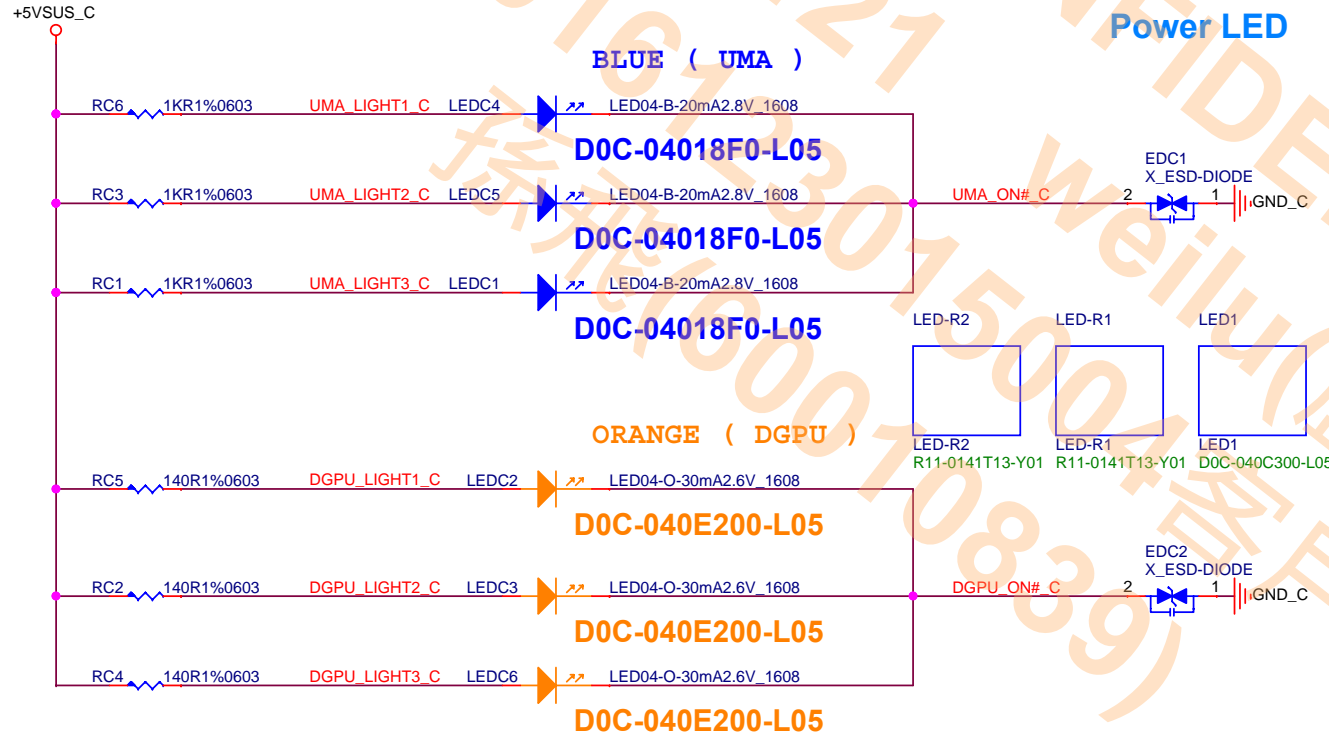
Diff Side Connector



DGPU Logic



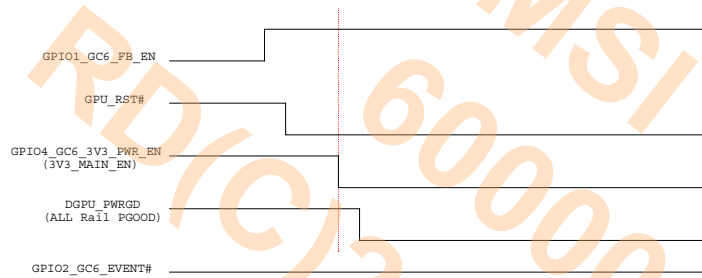
Power LED



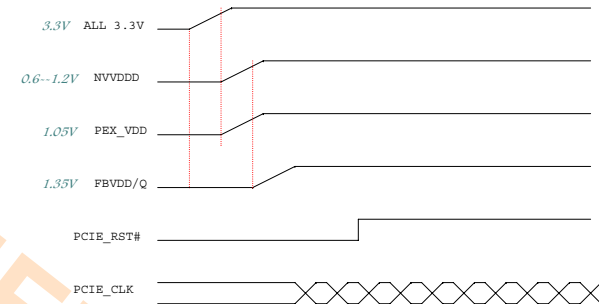
msi MICRO-STAR INT'L CO.,LTD.	
Title Power SW Board	
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MS-16H8 DGPU POWER SEQUENCE

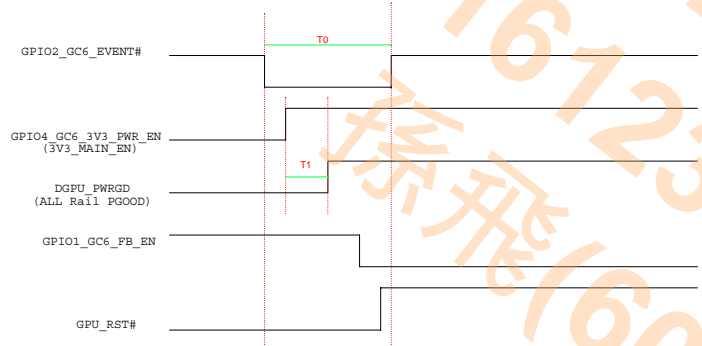
GC6 2.0 ENTRY SEQUENCE



GPU POWER ON SEQUENCE



GC6 2.0 EXIT SEQUENCE



NOTES:

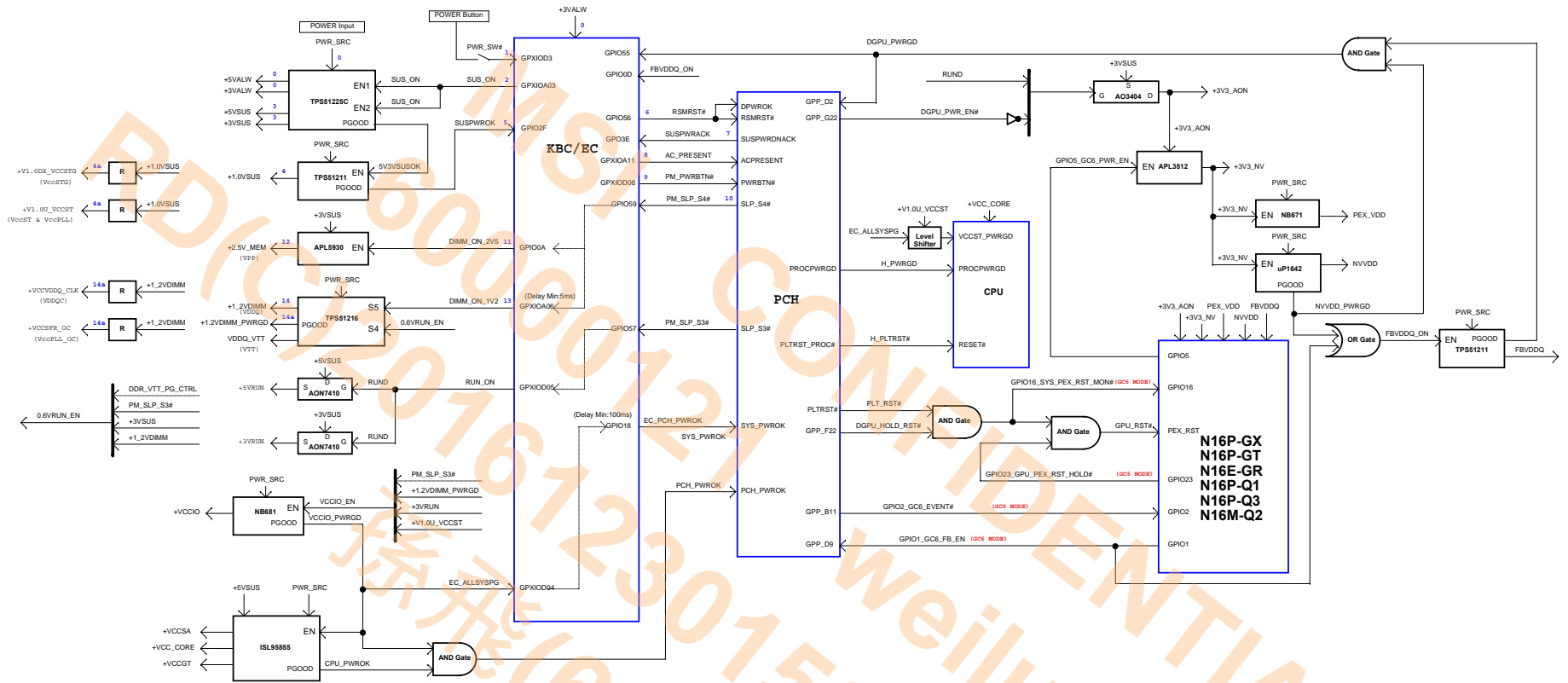
1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltage.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

GC6 2.0 TIMING

	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU_EVENT# assertion
T1	0.04	4	ms	3V3_MAIN_EN assertion to all power rails up and stable

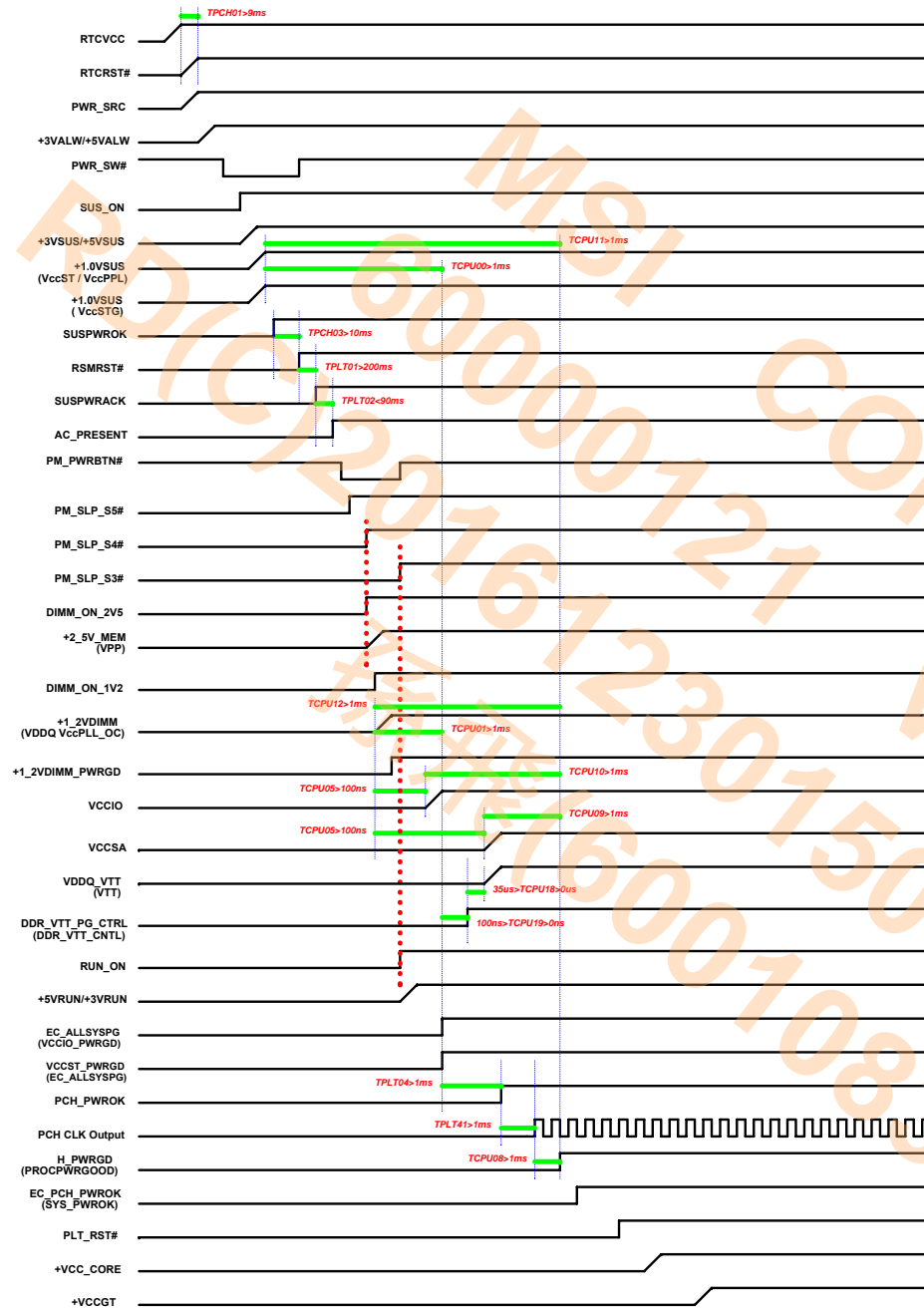
NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

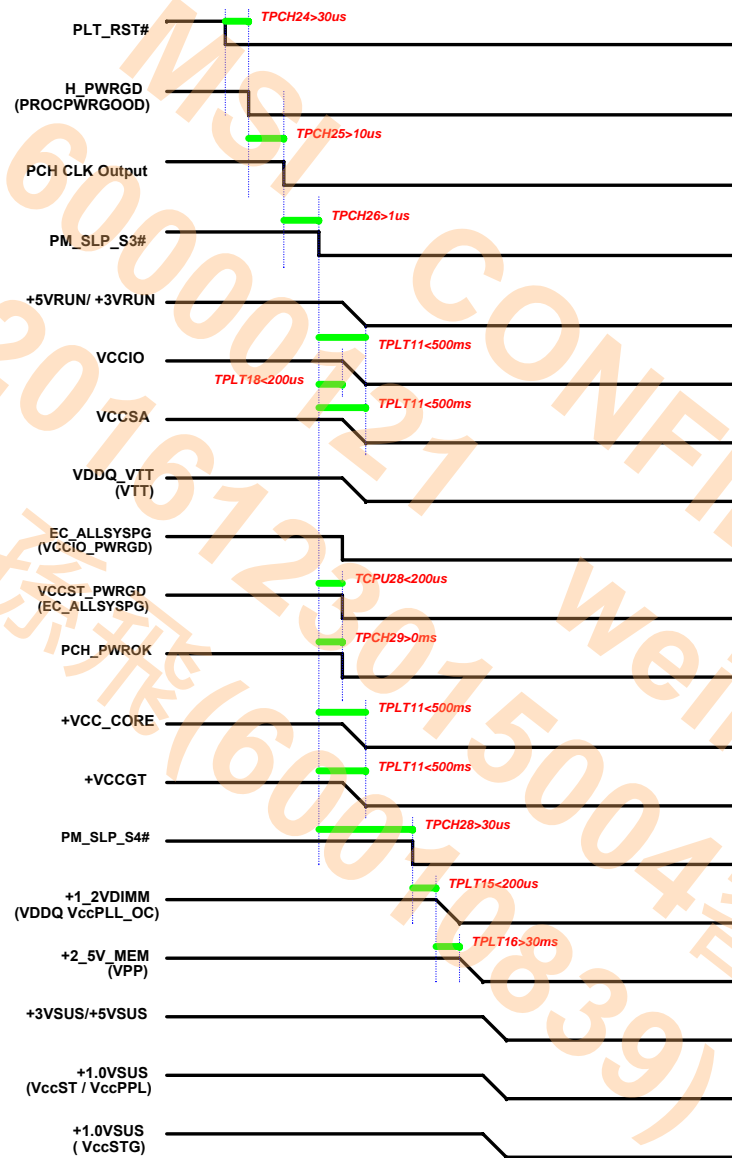


Power On Sequence

G3 -> S0




S0 -> G3



History

MSI
60000121
RD(C)2016123015004
weilu(盧偉)
孫飛(60010839)
客戶服務部

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Title			
History			
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